Nokia Customer Care
NHL-12 Series Transceivers

6 - Baseband Description & Troubleshooting

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1. Glossary of Terms

A/D	Analog to Digital
ACI	Accessory Interface
AFC	Automatic Frequency Control
APE	Application Program Engine
ASIC	Application Specific Integrated Circuit
BSI	Battery Size Indicator
BT	Bluetooth
BTEMP	Battery Temperature
CBUS	Nokia Proprietary Serial Interface for MCU
CDMA	Code Division Multiple Access
CMT	Cellular Mobile Telephone
D/A	Digital to Analogue
DAC	Digital to Analogue Converter
DAI	Digital Audio Interface
DBUS	Nokia Proprietary Serial Interface for DSP
DC	Direct Current
DCT	Digital Core Technology
DMA	Direct Memory Access
DSP	Digital Signal Processor
EMC	Electro Magnetic Compatibility
FBUS	Nokia Proprietary Serial Interface
FM	Frequency Modulation
FMEA	Failure Mode and Effect Analysis
GSM	Global System for Mobile Communications
Helen	Processor from Texas Instruments (also called OMAP1510)
HF	Hands Free
HFCM	Hands Free Common Mode
HW	Hardware electronics including Audio, Energy Management, UIHW and BB
I2C	Inter-IC Control bus

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IC	Integrated Circuit
IF	Interface
IHF	Integrated Hands Free
IMEI	International Mobile Equipment Identity
IO, I/O	Input Output
LCD	Liquid Crystal Display
LDO	Low Drop Out
LED	Light Emitting Diode
LSB	Least Significant Bit
LTPSi	Low Temperature Poly Silicon
MBUS	Nokia Proprietary Serial Interface
MCU	Micro Controller Unit
MMC	Multi Media Card
MMU	Memory Management Unit
MPU	Micro Processing Unit
MSB	Most Significant Bit
NTC	Negative Temperature Coefficient
PS	Power Save signal
PURX	Power Up Reset
PWB	Printed Wiring Board
PWM	Pulse Width Modulation
RF	Radio Frequency
RTC	Real Time Clock
SDRAM	Synchronous Dynamic Random Access Memory
SIM	Subscriber Identity Module
SMPS	Switch Mode Power Supply
SW	Software
TFT	Thin Film Transistor
TI	Texas Instruments
uBGA	Micro Ball Grid Array package
UEM	Universal Energy Management

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UI	User Interface
UPP	Universal Phone Processor
USB	Universal Serial Bus
VBAT	Battery Voltage
VCTCXO	Voltage Controlled
VGA	Video Graphics Array
XBUS	Proprietary Nokia serial communication bus

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2. Baseband Top-Level Description

NHL-12 is an imaging category (IP2.5) phone introducing a high-quality colour LCD, improved camera and EDGE for Americas. NHL-12 operates on triple-band GSM (850/1800/1900) and E-GPRS networks, and supports enhanced interfaces for connectivity with BT (Bluetooth) and USB (Universal Serial Bus).

The NHL-12 baseband consists of a dual-processor engine and some product specific blocks, such as IrDA and S60-display.

NHL-12 hardware and baseband consist of two parts: application part APE and phone part CMT.

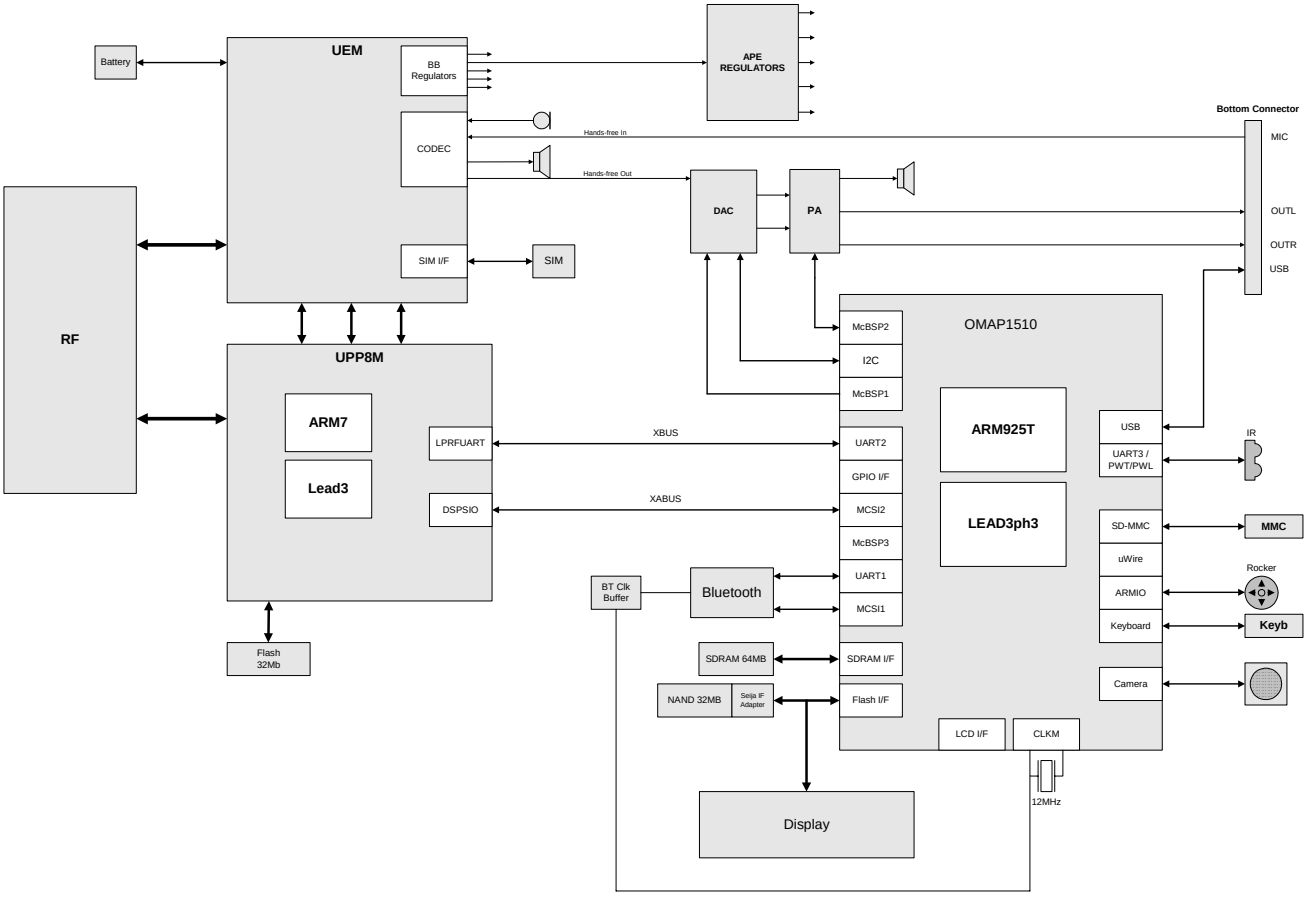
The APE part is constructed around an OMAP 1510 processor with SDRAM and NAND flash memory as the core. Other major parts for APE are power, UI, audio, Bluetooth and camera.

APE and CMT parts are connected by serial communication buses and by a few control lines. APE part reset and power control comes from the CMT side. Audio control is mostly performed on the APE side, and phone audio is routed from the CMT side.

Baseband block diagram

The below system block shows the main BB function blocks.

Figure 1:Baseband block diagram



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Environmental specifications

Normal and extreme voltages

- Nominal voltage:3.7V
- Lower extreme voltage:3.1V
- Higher extreme voltage:4.2V

Humidity

Operational humidity range is < 95%. Condensed or splashed water may cause interim or permanent phone malfunction.

Table 1: Operational conditions

Environmental condition	Ambient temperature	Notes
Normal operation	-10 ^{o}C... +55 ^{o}C	Specifications fulfilled
Reduced performance	+55 ^{o}C... +75 ^{o}C -25^{o}C... -10 ^{o}C	Operational only for short periods
No operation	-40 ^{o}C... -20 ^{o}C	Operation not possible but an attempt to operate will not damage the phone
No operation or storage	< -40 ^{o}C and > +85 ^{o}C	No storage; an operation attempt may cause permanent damage
Charging allowed	-25 ^{o}C... +60 ^{o}C	
Long term storage conditions	0 ^{o}C... +40 ^{o}C	

Frequencies in baseband

Table 2: CMT clocks

Function	Clock speed	Location	On/Off
VCTCXO	26 MHz	VCTCXO/HELGO	DSP/MCU is awake all the time.
System Clock	13 MHz	UPP	DSP/MCU is awake all the time.
DSP	195 MHz	UPP	DSP is awake all the time.
MCU	50.38 MHz	UPP	MCU is awake all the time.
Sleep clock	32.768 kHz	UEM – UPP - OMAP	During sleep mode

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Table 2: CMT clocks

Function	Clock speed	Location	On/Off
Cbus	1 MHz	UPP–UEM/Zocus Interface	Generated continuously whilst MCU is awake
Dbus	13 MHz	UPP/UEM Interface	During transceiver activity
RFConvClk	13 MHz	UPP/UEM Interface	During transceiver activity
RFBusClk	13 MHz	UPP/HELGO Interface	During transceiver activity
Flash	50.38 MHz	UPP/Flash Interface	Burst read accesses
SIM	3.25 MHz	UPP/SIM Interface	SIM accesses

Table 3: APE clocks

Function	Clock Speed	Source	To	Parameter
APE system clock	12 MHz	Crystal	OMAP1510	Frequency
OMAP DSP	150 MHz	OMAP Internal	DSP clock	Frequency
OMAP MCU	150 MHz	OMAP Internal	MCU clock	Frequency
CLK32K_IN	32768 Hz	UEM	OMAP1510 Sleep mode	Frequency
Flash interface	37.5 MHz	OMAP	Flash – APE	Frequency
SDCLK	75 MHz	OMAP	SDRAM – APE	Frequency
BT	12 MHz	Crystal	BT module	Frequency
MMC_CLK	16 MHz	OMAP	MMC	Frequency
SCLK	12 MHz	OMAP	Audio DAC	Frequency
Camera clock	12 MHz	OMAP	Camera	Frequency

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3. Baseband Architecture

CMT side

The CMT architecture is based on DCT4 Common Baseband.

The main functionality of the CMT baseband is implemented into two ASICs: UPP (Universal Phone Processor) and UEM (Universal Energy Management).

System clock for the CMT is derived from the RF circuits. For the CDMA system, the RF clock is 19.2 MHz and for GSM it is 26 MHz. The low frequency sleep clock is generated in the UEM using an external 32.768kHz crystal. The I/O voltage of the CMT baseband is 1.8V. The analogue parts are powered from 2.8V power rails. The core voltage of UPP can be altered with SW, depending on the prevailing processing power requirements.

UEM is a dual voltage circuit. The digital parts are running from the baseband supply (1.8V) and the analogue parts are running from the analogue supply (2.8V). Some of the UEM blocks are also connected directly to the battery voltage (VBAT). UEM includes 6 linear LDO (low drop-out) regulator for baseband and 7 regulators for RF. It also includes 4 current sources for biasing purposes and internal usage. Some parts of the SIM interface have been integrated into UEM. The SIM interface supports 1.8V and 3V SIM cards. Data transmission between the UEM and UPP is handled via two serial buses: DBUS for DSP and CBUS for MCU. There are also separate signals for PDM coded audio. Digital speech processing is handled by the DSP inside UPP and the audio codec is in UEM.

The analogue interface between the baseband and the RF sections is implemented into UEM. UEM provides A/D and D/A conversion of the in-phase and quadrature receive and transmit signal paths and supplies the analogue TXC and AFC signals to the RF section under the UPP DSP control. The digital RF-BB interface, consisting of a dedicated RFIC control bus and a group of GenIO pins, is located in UPP.

The baseband supports both internal and external microphone inputs and speaker outputs. Input and output signal source selection and gain control is done in the UEM according to control messages from the UPP. Keypad tones, DTMF and other audio tones are generated and encoded by the UPP and transmitted to UEM for decoding.

NHL-12 has two galvanic serial control interfaces for CMT: FBUS and MBUS.

Communication between the APE and CMT parts is handled through two serial buses: XBUS and XABUS. XBUS is the main communication channel for general use, and XABUS is for audio data transfer. Also the system reset (PURX) and SleepClk for APE are coming from the CMT side. The PURX is delayed approximately 130ms to fulfil OMAP1510 reset timing requirements and one of UEM's IR level shifters is used for SleepClk level shifting.

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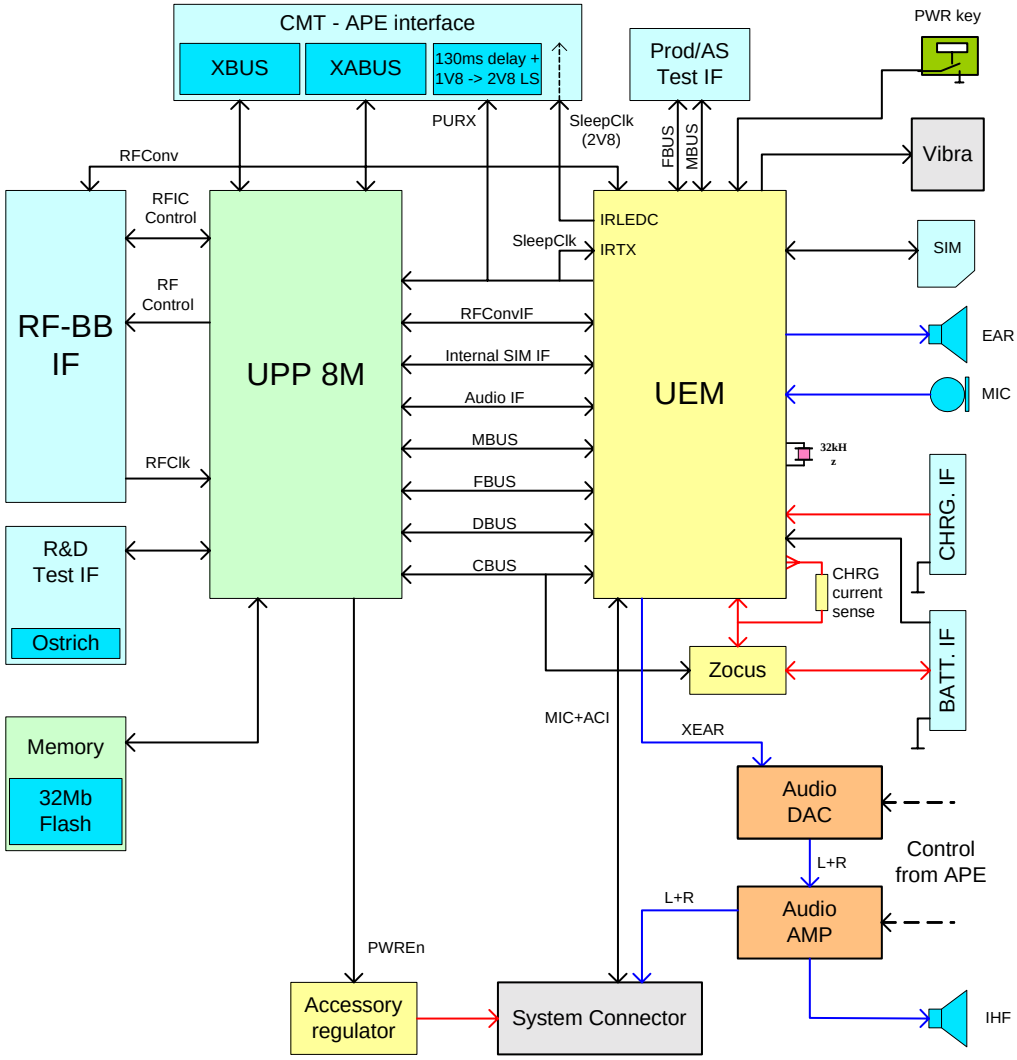
Figure 2:Simplified block diagram for CMT side



CMT memories

The memory interface supports 16-bit burst mode NOR FLASH with multiplexed address/data bus, standard asynchronous 8-bit SRAM and 16-bit address/data multiplexed SRAM. The UPP has two dedicated CS pins for FLASH and one GenIO that can be used as RAM CS.

The maximum amount of 16-bit SRAM with multiplexed address/data bus that can be connected to UPP is 2MBytes.

Memory configuration

The maximum amount of memory supported by UPP is 2*16MBytes of FLASH plus 2MBytes of external SRAM.

CMT memory configuration includes 32Mbits of 54MHz NOR FLASH. The flash has read-while-write capabilities.

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APE side

The functionality of the APE engine is based on the OMAP1510 processor and memories. APE has a total of 32 Mbytes of NAND type flash memory and 64 Mbytes of SDRAM.

The application engine has two separate clock sources: one for the system clock (12MHz) and one for the sleep clock (32.768kHz), which is called Clk32k. The Clk32k is not generated by the application engine, but is derived from the CMT SleepClk using a level shifter. The Clk32k is always running when the engine is powered.

The 12MHz system clock is generated by OMAP1510. The crystal driver and related circuitry is internal to the processor and an external quartz crystal is used as a frequency reference. The Bluetooth clock is also derived from this clock using a clock buffer. Note that the system clock is switched off during sleep mode.

The APE reset (MPU_nReset) is controlled by the CMT reset (PURX) generated by UEM. PURX and MPU_nReset have different logic levels, but the latter is not simply a level shifted version of the former. There is also an external delay circuit connected between the PURX and MPU_nReset lines that keeps the APE reset active circa 130ms after CMT reset is released.

OMAP1510 consists of:

- DSP megamodule with internal program and data memory, instruction cache, DMA controller and hardware accelerator
- ARM925T based processor megamodule with memory management unit (MMU), instruction and data cache
- local bus with MMU
- multi-channel system DMA controller
- peripherals (local and shared) that support glueless system interface
- connecting modules that facilitate communication between these megamodules and system memory (external and internal), and enhance system's throughput and software development.

OMAP 1510 is optimized for various multimedia and wireless applications such as wireless video and image processing, wireless audio applications, graphics and video display acceleration.

APE memories

APE memory system consists of a 64Mbyte(32Mx16) SDRAM device connected to the OMAP1510 fast external memory interface (EMIFF) and a 32Mbytes(32Mx8) of NAND-flash device connected via Seija Flash-Interface Adapter ASIC to the OMAP1510 slow external memory interface, EMIFS. The memory interface is shown in Figure 3, "APE external memories," on page 14. NAND-flash is used as a boot the device and mass memory. User data is stored in NAND. The operating voltage of all memory components is 1.8V, supplied from V18.

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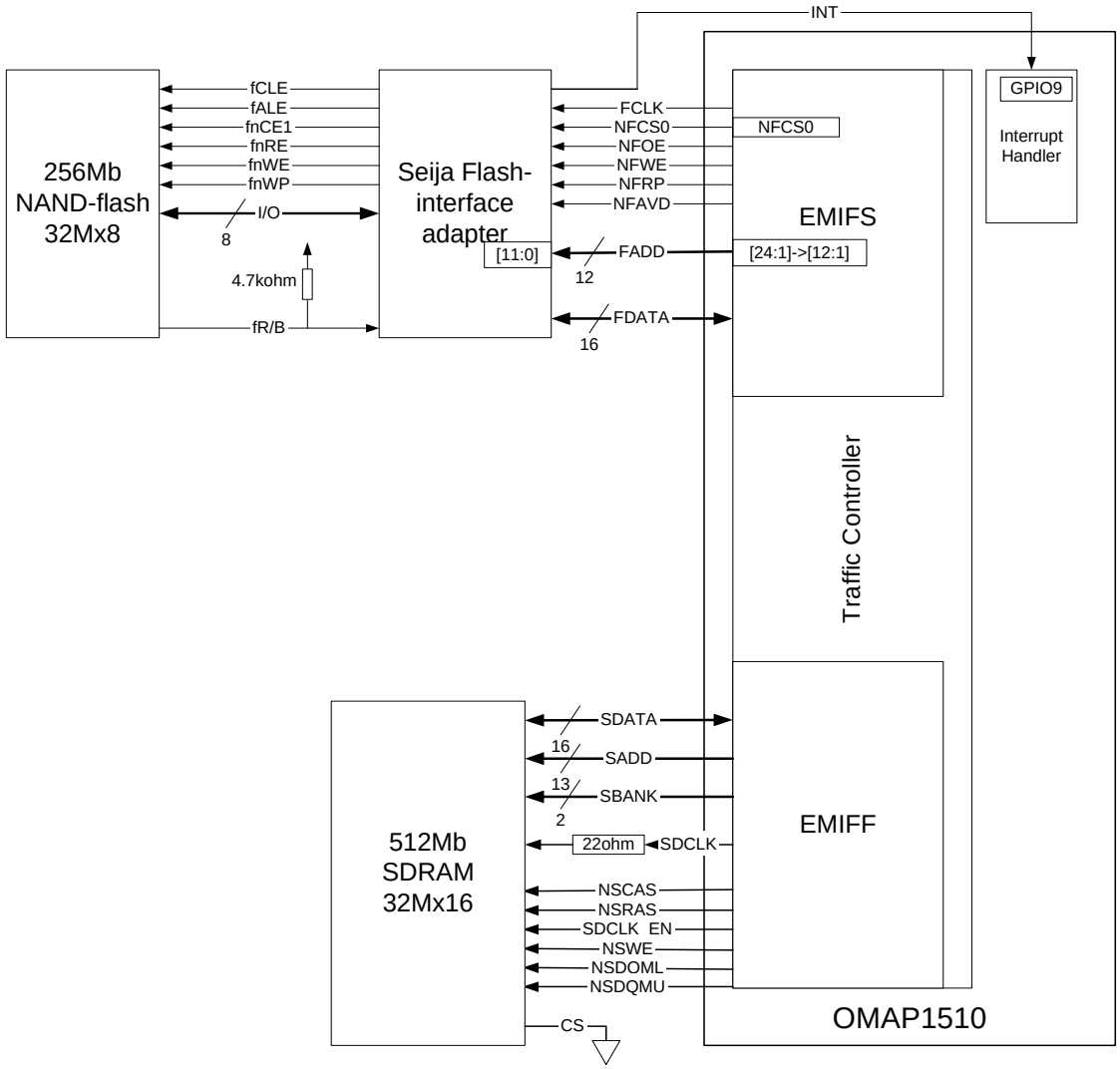
Figure 3: APE external memories



Memories are packaged as follows:

- SDRAM, 54ball CSP, 10x11.5x1.1mm, 0.8mm pitch Pb-free balls
- NAND, 63ball TBGA, 11x9x0.9mm, 0.8mm pitch Pb-free balls
- Seija ASIC, 64ball FBGA, 6x6x1.2mm, 0.5mm pitch Pb-free balls

Energy management

The energy management of NHL-12 is based on BB 4.0 architecture. BL-5C battery supplies power primarily to the UEM ASIC and the RF PA. UEM includes several regulators to supply RF and baseband. It provides the energy management including power up/down procedure.

Power supply modes

The state machine in UEM controls mainly the operating modes of the engine. State transitions are enabled by signals taken from UEM, UPP and OMAP1510. In general, the state transitions are based on the following information:

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- Battery voltage (HW limits and cutoffs)
- Back-up battery voltage limits and cutoffs
- Power key status (in NHL-12 engine power key connected to PWRONX pin of UEM)
- Delays generated by the state machines
- Real time clock (RTC) alarms
- Watchdogs
- Thermal shutdowns
- SLEEPX signal from UPP
- LOW_PWR signal from OMAP1510

The functional behaviour of the UEM can be divided into 6 different states. Since the UEM controls the regulated power distribution of the phone, each of these states affects the general functionality of the phone:

- No supply
- Backup
- Power off
- Reset
- Power on
- Sleep

Brief description of operating modes

- NO_SUPPLY mode means that the main battery is not present or its voltage is too low (below UEM master reset threshold limit) and back-up battery voltage is too low.
- In BACK_UP mode the main battery is disconnected or empty but back-up battery has sufficient charge in it
- IN POWER_OFF mode the main battery is present and its voltage is over UEM master threshold limit. All regulators are disabled.
- RESET mode is a synonym for start-up sequence and contains in fact several modes. In this mode certain regulators and system oscillators are enabled and after they have stabilized, the system reset (PURX) is released and PWR ON mode entered.
- In POWER_ON mode SW is running and controlling the system.
- SLEEP mode is entered only from PWR ON mode when system activity is low. CMT and APE sides can be in sleep mode independent of each other.

For controlling transitions between modes, UEM includes:

- RC oscillator (32kHz)
- crystal oscillator (32kHz)
- comparators

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- digital circuitry

These are used for generating limits and time delays.

Controlled powering off is done when the user requests it or when the battery voltage is falling too low. Complete power down is done, if SW does not write to the watchdog register anymore and a defined time after previous writing is elapsed. As this happens, PURX is forced low and all regulators are disabled. If the battery voltage falls below the very last SW–cutoff level, SW will power off the system by letting the UEM's watchdog elapse. If a thermal shutdown limit in UEM regulator block is exceeded, the system is powered off. System reset PURX is forced low.

Uncontrolled powering off happens, when the battery is suddenly removed. This is problematic as data may corrupt in memories, if the removal takes place during the access phase to these devices. UEM's state machine notices battery removal after battery voltage has been below VCOFF– for 5 us and enters PWR_OFF mode. PURX is set low and all UEM's regulators are disabled.

There are three watchdogs in UEM. First one is for controlling system power-on and power-down sequences. The initial time for this watchdog after reset is 32s. The time can be set using a register. This watchdog is used for powering the system off in a controlled manner. The second one is for security block and is used during IMEI code setting. The third one is a power key watchdog. It is used to power off the system in case SW is stuck and the user presses the power key. This watchdog, if not acknowledged by the SW, shuts down the system after a predefined delay (2–15 seconds). The feature is enabled as default and can be disabled by SW.

OMAP1510 also includes a hardware watchdog. This resets OMAP1510, BT and Seija at the same time. It is possible to disable this watchdog with the help of SW.

Table 4: Reset thresholds and cutoff limits

VMSTR+	Master reset threshold	2.1 V
VMSTR–	Master reset threshold	1.9 V
VCOFF+	Hardware cutoff	3.1 V
VCOFF–	Hardware cutoff	2.8 V
VCHAR+	VCHAR detection threshold	2.0 V
VCHAR-	VCHAR detection threshold	1.8 V
SW_{CUTOFF}	SW cutoff limit	System dependent
VBUCOFF+	Backup battery cutoff	2.1 V
VBUCOFF–	Backup battery cutoff	2.0 V

Battery BL-5C

The main battery of NHL-12 is a lithium ion battery BL-5C with the capacity of 850mA.

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The battery interface has three pins: VBAT, GND and BSI. Temperature indication is located on the engine PWB. Temperature measurement is performed using an NTC resistor (47k nom) on the engine PWB.

Current gauge (Zocus)

The NHL-12 engine supports HW for phone and charging current measuring. The current measurement chip that is used is LM3820. Current gauge is also supported by the ISA EM Core SW. It can be used to estimate the battery charge level presented as battery bars on the display.

Current is measured from the positive battery terminal using a sense resistor, so that all phone's consumed current flows through that resistor. Correspondingly, when charging, all current to phone's battery flows through this resistor, but the direction is reversed. The sense resistor is formed from PWB tracks arranged as a 4-terminal resistor. LM3820 senses voltage across the resistor. The maximum current depends on the sense resistor value.

RTC capacitor

Real Time Clock (RTC), crystal oscillator and backup battery circuitry are located inside the UEM. Two regulators are used to provide needed voltages for external backup supply and backup battery charging: VRTC for internal clock circuitry and VBU for backup battery charging. The backup battery has voltage range VBACK = $2.0V_{min}$ – $3.2V_{typ}$ – $3.3V_{max}$ (charged to 3.2V and discharged down to 2.0V).

Charging the backup battery is controlled by the UEM's digital block by enabling VBU regulator and backup battery is charged with constant voltage up to 3.2V. By default, VBU regulator is disabled in reset and it is reset always when PURX='0'.

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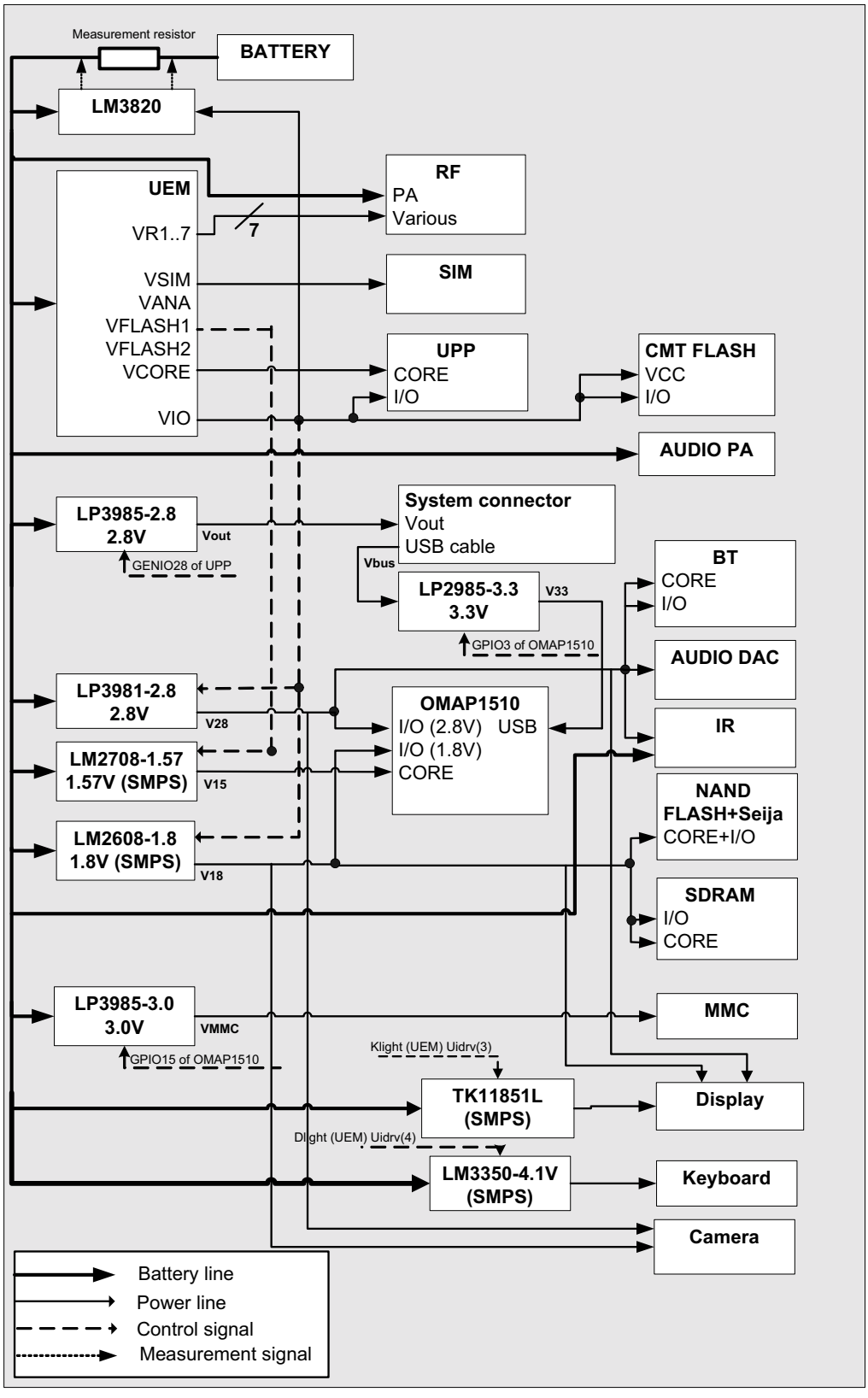
Power distribution

Figure 4: Power distribution diagram



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DC characteristics

Regulators

The transceiver baseband section has a multi-function analogue ASIC, UEM, which contains six pieces of 2.78 V linear regulators and a 4.8 V switching regulator. All the regulators can be controlled individually by the 2.78 V logic directly or through a control register.

The seven regulators are named VR1 to VR7. VrefRF01 and VrefRF02 are used as the reference voltages for Helgo, VrefRF01 (1.35V) for the bias reference and VrefRF02 (1.35V) for the Rx ADC (analog-to-digital converter) reference.

The regulators (except VR7) are connected to Helgo. Different modes of operation can be selected inside Helgo according to the control information coming through the RFBus. UEM's internal regulators are used for the powering of the baseband module. In addition to this, VIO and VFLASH1 regulators of UEM are used to enable/disable APE side regulators.

VCORE and VSIM are programmable linear regulators. Default state for VCORE voltage is 1.57V.

There are also internal regulators in UEM. They are used for the powering of the CMT BB. In addition to this, VIO and VFLASH1 regulators of UEM are used to enable/disable APE side regulators. BB4.0 supports only UEMKEdge or UEMC with UPP8Mv3.

NHL-12 APE energy management uses two switch mode power supplies: LM2608 and LM2708, generating 1.57V and 1.8V to OMAP1510 and memories. In addition, the APE side EM HW consists of several other discrete regulators:

- One linear regulator for 2.8V APE side logic (LP3981)
- One 2.8V linear regulator (LP3985) for powering the MMC card.
- One 3.3V linear regulator (LP2985) for powering the USB block of OMAP1510.

LM2608 is used to generate 1.8V for I/O's OMAP1510 processor and APE side memories. Normally, LM2608 works in constant frequency PWM mode. But in the case of light loads, it is possible to control LM2608 via SYNC/MODE pin to low quiescent current mode. In this mode, LM2608 works as a linear regulator and the output current capacity is only 3mA. LM2608 needs an external 1.35V reference voltage. In the case of NHL-12 engine, this reference voltage is taken from VrefRF01 of the UEM.

LM2708 is used to generate 1.57V for the core of OMAP1510 processor. LM2708 does not need external reference voltage. Pin (Isel) can be used to adjust the current limit external coil. NHL-12 engine has a higher current limit, which allows 400mA output current capacity.

In NHL-12 engine, LOW_PWR signal of OMAP1510 (multiplexed on pin ARMIO_5) is used to control LM2708/LM2608 to linear mode when processor goes to deep sleep mode. The functionality of the LOW_PWR signal is the following: when OMAP1510 is in a low power state (deep sleep mode), this signal is high. At reset and when in normal functional mode, this signal is low. Because the polarity SYNC/MODE pin is reverse, an additional inverter is used in this control line.

Table 5: CMT regulators

Regulator	Min Voltage V	Nom. Voltage V	Max.Voltage V	Max. Current mA
VIO	1.72	1.8	1.88	150

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Table 5: CMT regulators

Regulator	Min Voltage V	Nom. Voltage V	Max.Voltage V	Max. Current mA
VCORE		1.053 1.35 1.57 1.8		200
VFLASH1	2.70	2.78	2.86	70
VFLASH2	2.70	2.78	2.86	40
VANA	2.70	2.78	2.86	80
VSIM	1.745 2.91	1.8 3.0	1.855 3.09	25

Table 6: APE regulators

Regulator Output	Type	Regulator Type	Main Voltage V	Min Voltage V	Max Voltage V	Max Current mA	Enabled by	Used for Block
V15	SMPS mode	LM2708-1.57	1.523	1.57	1.617	400	VFLASH 1	OMAP Core
	Linear mode		1.282	1.35	1.418	15		
V18	SMPS mode	LM2608-1.8	1.764	1.8	1.836	400	VIO	OMAP I/O, SDRAM Core+I/O, NAND Flashes+ Seija, LCD, camera
	Linear mode		1.710	1.8	1.890	3		
V28	Linear	LP3981-2.8	2.716	2.8	2.884	300	VIO	OMAP I/O, BT Audio DAC, LCD, cam-era, IR
VMMC	Linear	LP2985ITLX-3.0	2.91	3.0	3.09	150	GPIO15	MMC
V33	Linear	LP2985-3.3	3.201	3.3	3.399	150	GPIO3	Helen USB

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Table 6: APE regulators

Regulator Output	Type	Regulator Type	Main Voltage V	Min Voltage V	Max Voltage V	Max Current mA	Enabled by	Used for Block
USB host		-	4.3	5.0	5.25	100		USB Regulator Input range
VOUT	Linear	LP3985-2.8	2.716	2.8	2.884	150	GENIO28	Accessory powering
V15	SMPS mode	LM2708-1.57	1.523	1.57	1.617	400	VFLASH1	OMAP Core
	Linear mode		1.282	1.35	1.418	15		
V18	SMPS mode	LM2608-1.8	1.764	1.8	1.836	400	VIO	OMAP I/O, SDRAM Core+I/O, NAND Flashes+ Seija
VKEYB	SMPS mode	LM3353NOPB	4.038	4.1	4.161	80mA	UEM Klight	Keypad leds

Voltage regulators in BB for RF

Values are referenced to GND unless otherwise specified.

Table 7: Voltage regulators in BB for RF

Signal	Min	Nom	Max	Note
VR1A / VR1B	4.6V	4.75V	4.9V	I_{max} = 10mA
VR2	2.70V	2.78V	2.86V	I_{max} = 100mA
VR3	2.70V	2.78V	2.86V	I_{max} = 20mA
VR4	2.70V	2.78V	2.86V	I_{max} = 50mA I_{sleep} = 0.1mA
VR5	2.70V	2.78V	2.86V	I_{max} = 50mA I_{sleep} = 0.1mA
VR6	2.70V	2.78V	2.86V	I_{max} = 50mA I_{sleep} = 0.1mA
VR7	2.70V	2.78V	2.86V	I_{max} = 45mA

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Table 7: Voltage regulators in BB for RF

Signal	Min	Nom	Max	Note
VrefRF01	1.334	1.35	1.366	Reference voltage Imax = 0.1mA
VrefRF02	1.323	1.35	1.377	Reference voltage Imax = 0.1mA

Charging

Charging control and charge switch are located in the UEM.

There is a thermal protection circuitry in the UEM to protect the chip. If temperature rises above the threshold(150×C typ.), a charge switch is opened immediately and charging is stopped. When the chip cools down, charging is continued normally.

HW supports all DCT4 chargers. 3-wire chargers are supported, but 3-wire charging is not. In practice this means that the 3-wire chargers are internally connected (charger control wire connected to GND) as 2-wire chargers.

Audio circuitry

This section describes the audio HW of the engine. External audio components and acoustics are not considered in detail in this section.

As this engine is based on dual-processor architecture, also audio is divided into separate APE and CMT parts. Audio control is mostly on the APE side; phone audio is routed from the CMT side to APE in analogue form, except Bluetooth which is in digital form. On the CMT side, audio HW is integrated into the UEM ASIC. On the APE side, the most important parts are OMAP1510, audio DAC and audio power amplifier.

The stereo output of this amplifier is designed for use with the extended Pop-port^{TM} connector. It also has a differential mono output for driving the handsfree speaker.

The battery voltage (VBATT) is used directly as supply voltage for audio amplifier. The nominal battery voltage is 3.6V.

The type of DAC used is TLV320AIC23B and the supply voltage for this is coming from V28.

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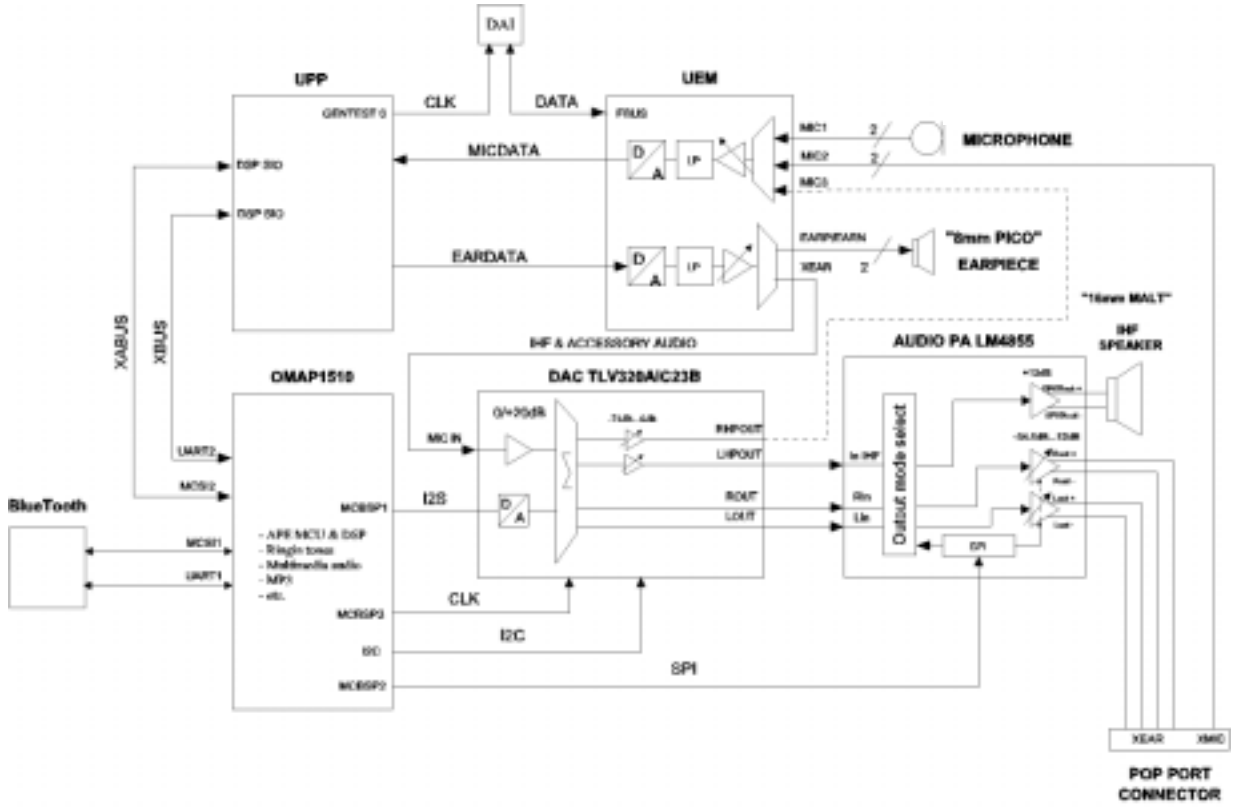
Figure 5:NHL-12 audio block diagram



Earpiece

NHL-12 uses an earpiece which is a 32 ohm speaker with a diameter of 8 mm. The supply voltage is 2.7V. The earpiece is driven differentially directly by the UEM. The capsule is mounted into the LCD frame assembly.

Internal microphone

The internal microphone is mounted in the B-cover. The microphone is omnidirectional and it is connected to the UEM microphone input MIC1P/N. The microphone input is asymmetric and the UEM (MICB1) provides the bias voltage. Nominal impedance of the microphone is 1.8kOhms. The microphone input to UEM is ESD protected. Spring contacts are used to connect the microphone to the main PWB.

Integrated hands-free

Integrated hands-free speaker (IHF), 16mm, is used to generate alerting and warning tones in NHL-12. The IHF speaker is driven with audio amplifier. The speaker capsule is mounted in the antenna module. Spring contacts are used to connect the IHF speaker contacts to the main PWB.

Audio accessory receive path

In NHL-12 the accessory receive path is directly driven from the UEM HF / HFCM differential audio outputs. The output signal complies with the Pop-port accessory interface.

For EMC protection, ferrites are connected in series to the earpiece and for ESD protection bizener is used.

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Audio control signals

The HEADINT signal is needed for recognizing the external device (e.g. headset) connected to the system. The recognition is based on the ACI-pin on the system connector.

The button of the external device generates HOOKINT. This is used, for example, to answer or to end a phone call.

Acoustics

Earpiece acoustics

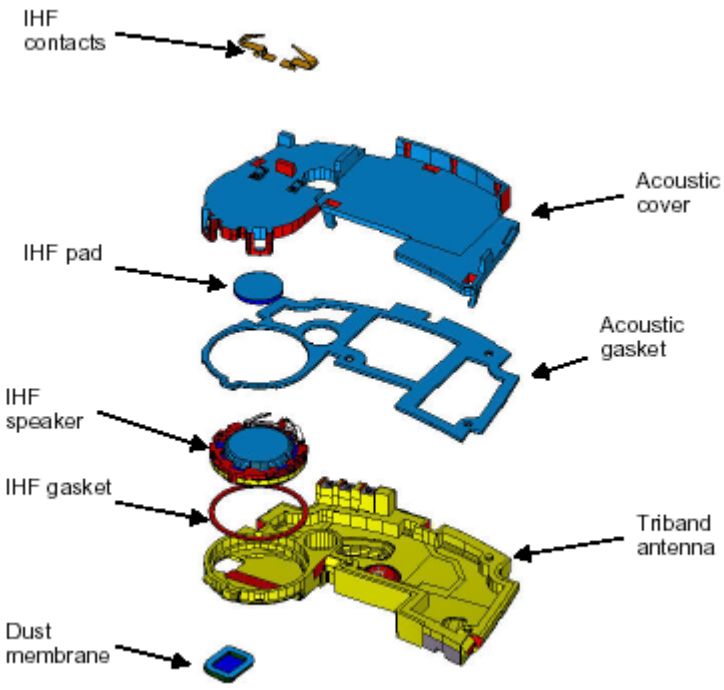
The earpiece is a PSS 8mm element. The earpiece is placed inside the plastic UI frame. It is sealed to UI support frame with a foam ring. This cavity is ported to a second cavity formed between the UI support frame and A-cover with Bezel. Sound holes vent this cavity out of the UI support flame. All holes are shielded to prevent dust and small particles from entering the phone.

IHF speaker acoustics

In NHL-12, the IHF speaker is used for integrated hands-free and ringing tone applications. It has a structure, which consists of two cavities: one back cavity and one front cavity.

When using the phone in the IHF mode, speech is fed to the IHF-speaker. Ringing tones are optimized according to bandwidth and frequency response. The sound holes are placed in the B-cover. Sound holes are shielded to prevent dust and small particles from entering the phone.

Figure 6:Exploded view of antenna assembly.



Microphone acoustics

NHL-12 has a standard microphone module. The module is embedded into a so-called "rubber boot" and connected to the system module by spring contacts.

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The microphone is placed close to the system connector. The sound port of the microphone is located towards the bottom of the phone.

Vibra motor

A vibra alerting device is used to generate a vibration signal for an incoming call. It is located in the middle part of the phone and it is connected to the main PWB with spring contacts. The vibra is controlled by a PWM signal coming from UEM. The vibra motor is mounted in the B-cover assembly.

Audio modes

This section describes NHL-12's engine audio modes. The following audio modes are supported:

- Hand portable
- Integrated hands-free
- Accessory audio mode
- APE audio mode
- Bluetooth audio mode

Hand portable

Hand portable mode is the basic audio mode. This is entered when no audio accessories are connected and the hands-free mode is not selected.

In the hand portable mode, earpiece path and internal microphone path are in use.

A call is created by the CMT. The uplink signal is generated by the microphone and transferred to MIC1P/N differential inputs. The internal microphone is enabled using the MICB1 bias voltage O/P on UEM. The signal is amplified at least by 20 dB, low pass filtered, converted into digital domain and then postponed through UPP to transducer equalizer and finally to APE for speech encoding.

The EAR output on the UEM is selected for Rx audio via the internal earpiece. The UEM sets the audio uplink gain and downlink attenuation. Different downlink attenuation levels function as the volume control.

The internal earpiece is driven by the CMT engine for voice calls. The internal microphone is driven by the CMT for voice calls and voice recording.

All volume controls are handled by the UEM.

Integrated hands-free audio mode (IHF)

This mode is entered by user selection.

A call is created by the CMT. The uplink signal is generated by the microphone and transferred to MIC1P/N differential inputs. The internal microphone is enabled using the MICB1 bias voltage O/P on the UEM.

The downlink audio is processed in the UPP and transferred to the UEM. Then the downlink signal is amplified in the single-ended XEAR Output driver in the UEM. The mono XEAR output is connected to the MICIN input of the APE Audio DAC via a low-pass filter. The signal is then routed through the line output of DAC (LHPOUT), high pass filtered and routed to the Phone_In_IHF input. This drives the internal speaker via the SPKRout driver.

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Accessory audio mode

This mode is entered when an audio accessory (mono/ stereo headset, loopset, basic car kit) is connected to the system connector. The routing of the audio signal is identical for all accessories (except for the stereo headset), but gain control depends on the accessory used.

The call is created by the CMT. The uplink signal is generated by the external microphone and transferred to the UEM MIC2 input, after which the MIC2B bias voltage and MIC2P/N inputs are enabled on the UEM.

The downlink audio signal is routed through the single-ended XEAR output driver by the UEM. The mono XEAR output is connected to the MICIN input of the DAC via a lopes filter. Then signal is routed through L_{OUT} and R_{OUT} drivers of DAC to the L_{IN} and R_{IN} inputs of the LM4855. Accessories are driven via the system connector using the L_{OUT} driver of LM4855. When a stereo headset is used also the R_{OUT} driver is connected. Both channels play the same mono audio signal.

APE audio mode

This mode is entered when a user starts a multimedia application (e.g. MP3, AAC etc.) or in the case of ringing tones/ other notification tones played via the IHF speaker or the system connector.

When an MP3 is played, encoded data is read from the MMC card and the decoding is performed by OMAP1510. After decoding, the raw linear data is sent to the external audio DAC as a 16-bit PCM audio through the I2S connection. The DAC performs the digital-to-analogue-audio conversion.

For playback and streaming of digital audio, synthesized ring tones, miscellaneous tones, and game sounds, the APE side can be selected to drive either the IHF speaker or the system connector.

For playback via the internal speaker, the LHPOUT output on the audio DAC is used. The signal is routed to Phone_in_IHF input on LM4855.

For playback via the stereo/ mono headset or other accessories, the L_{OUT} and R_{OUT} outputs of the Audio DAC are used. These are routed to the L_{IN} /R_{IN} inputs of the LM4855. In the case of mono accessory, OMAP1510 produces a monophonic signal to DAC.

Bluetooth audio mode

Bluetooth audio data is transferred using a separate interface, MCSI.

MCSI is a serial (voice) interface with multi-channels transmission capability. There are two independent MCSI interfaces in OMAP1510 and one of them, MCSI1, is connected to the PCM interface of BC02. The MCSI1 is a half-duplex interface and it can work as either master or slave. This 4-wire interface has a bi-directional serial clock and frame synchronization. MCSI has a programmable word length (from 3 to 16 bits) and frame configuration.

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4. Baseband External and Internal Signals and Connections

This section describes some of the external and internal electrical connections and interface levels on both CMT and APE side. The electrical interface specifications are collected into tables that cover a connector or a defined interface.

CMT internal signals and connections

Table 8: Internal microphone

Signal	Min	Nom	Max	Condition	Note
MICP			200mV$_{pp}$	AC	2.2kΩ to MIC1B
	2.0 V	2.1 V	2.25 V	DC	
MICN	2.0V	2.1V	2.25V	DC	

Table 9: Internal speaker

Signal	Min	Nom	Max	Condition	Note
EARP	0.75V	0.8V	2.0 V$_{pp}$ 0.85V	AC DC	Differential output (V$_{diff}$ = 4.0 V$_{pp}$)
EARN	0.75V	0.8V	2.0 V$_{pp}$ 0.85V	AC DC	

CMT external signals and connections

Table 10: DC connector

Pin	Signal	Min	Nom	Max	Condition	Note
1	VCHAR		11.1V$_{peak}$	16.9 V$_{peak}$ 7.9 V$_{RMS}$ 1.0 A$_{peak}$	Standard charger	Charger positive input
		7.0 V$_{RMS}$	8.4 V$_{RMS}$	9.2 V$_{RMS}$ 850 mA	Fast charger	
2	CHGND		0			Charger ground

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Table 11: Pop-port™ connector

Pin	Signal	Description	Spectral range	U/I levels	Impedance	Notes
1	CHARGE	V Charge	DC	0-9 V / 0.85 A		
2	GND	Charge GND		0.85 A	100 mΩ	(PWB + conn.)
3	ACI	ACI	1 kbit/s	Dig 0 / 2.78V	47 Ω	Insertion & removal detection
4	VOUT	DC out	DC	2.78V / 70mA	100 mΩ	(PWB + conn.) 200mW
5	USB VBUS	DC in	DC	4.375-5.25V		Connected to APE side
6	USB D+		12M	0-3.3V		Connected to APE side
7	USB D-		12M	0-3.3V		Connected to APE side
8	USB Data GND	Data GND			Ferrite to engine GND	
9	XMIC N	Audio in	300 - 8k	1Vpp & 2.78V		DC
10	XMIC P	Audio in	300 - 8k	1Vpp & 2.78V		DC
11	HSEAR N	Audio out	20 - 20k	1Vpp	10 Ω	
12	HSEAR P	Audio out	20 - 20k	1Vpp	10 Ω	
13	HSEAR R N	Audio out	20 - 20k	1Vpp	10 Ω	Not conn. In mono
14	HSEAR R P	Audio out	20 - 20k	1Vpp	10 Ω	Not conn. In mono

Table 12: Electrical characteristics of SIM connector

Pin	Name	Parameter	Min	Typ	Max	Unit	Notes
1	VSIM	1.8V SIM Card	1.62	1.8	1.98	V	Supply voltage
		3V SIM Card	2.7	3.0	3.3	V	
2	SIMRST	1.8V SIM Card	0.8xVSIM 0		VSIM 0.2xV SIM	V	SIM reset (output)
		3V SIM Card	0.8xVSIM 0		VSIM 0.2xV SIM	V	

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Table 12: Electrical characteristics of SIM connector

Pin	Name	Parameter	Min	Typ	Max	Unit	Notes
3	SIMCLK	Frequency		3.25		MHz	SIM clock T_{rise}/T_{fall} max 50 ns
		T_{rise}/T_{fal}l			50	ns	
		1.8V V_{oh} 1.8V V_{ol}	0.7xVSIM 0		VSIM 0.2xV SIM	V	
		3V V_{oh} 3V V_{ol}	0.7xVSIM -0.3		VSIM 0.2xV SIM	V	
4	DATA	1.8V V_{oh} 1.8V V_{ol}	0.7xVSIM -0.3		VSIM 0.3	V	SIM data (output)
		3V V_{oh} 3V V_{ol}	0.7xVSIM -0.3		VSIM 0.3		
		1.8V V_{ih} 1.8V V_{il}	0.7xVSIM -0.3		VSIM +0.3 0.2xV SIM	V	SIM data (input) T_{rise}/T_{fall} max 1µs
		3V V_{il} 3V V_{il}	0.7xVSIM -0.3		VSIM +0.3 0.2xV SIM		
5	NC						Not connected
6	GND	GND	0		0	V	Ground

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5. BB-RF Interface

The interface between the baseband and the RF section is mainly handled by the UEM ASIC**.** UEM provides A/D and D/A conversion of the in-phase and quadrature receive and transmit signal paths and also A/D and D/A conversions of the received and transmitted audio signals to and from the user interface.

The UEM supplies the analogue TXC and AFC signals to the RF section according to the UPP DSP digital control. Data transmission between the UEM and the UPP is implemented using two serial busses: DBUS for DSP and CBUS for MCU. There are also separate signals for PDM coded audio. Digital speech processing is handled by the DSP inside UPP ASIC. UEM is a dual voltage circuit: the digital parts are running from the baseband supply 1.8V and the analogue parts are running from the analogue supply 2.78V; also VBAT is directly used.

The table below describes all the analogue signals from the baseband block to the RF block and back. The signal names are based on the schematics.

Table 13: Analogue signals between BB and RF

Signal Name	From	To	Parameter	Min	Typ	Max	Unit	Function
VCTCXO	VCTCXO	UPP	Frequency		26		MHz	High stability clock signal for the logic circuits, AC coupled. Distorted sinewave e.g. sawtooth.
			Signal amplitude	0.2		1.32	Vpp	
			BB load resistance	10			kohm	
			BB load capacitance			10	pF	
			DC level	1.3	1.35	1.4	V	
			Input impedance	500			kohm	
			DC level	1.17	1.20	1.23	V	
			Source impedance			200	ohm	
TXQP / TXQN	UEM	Helgo	Same spec as for TXIP / TXIN					

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Table 13: Analogue signals between BB and RF

Signal Name	From	To	Parameter	Min	Typ	Max	Unit	Function
AFC	UEM	VCTCXO	Voltage Min Max	0.0 2.4		0.1 2.55	V	Automatic frequency control svoltage for the VCTCXO
			Source impedance			200	ohm	
TXC	UEM	Helgo	Voltage Min Max	2.4		0.1	V	Transmitter power level and ramping control
			Source impedance			200	ohm	
			Load resistance capacitance	5		 15	kohm pF	
RFTemp	Helgo	UEM	Voltage at -20 deg.C		1,57		V	Temperature sensor of the RF.
			Voltage at +25 deg.C		1,7			
			Voltage at +60 deg.C		1,79			
DC_sense	PA	UEM	Voltage	0.7	1.35	2.0	V	PA final stage quiescent current level information
IPA1&IPA2	UEM	PA	Output voltage	0		2.7	V	PA final stage quiescent current adjustment
			Current range	0		5	mA	
			Resolution	4			bits	

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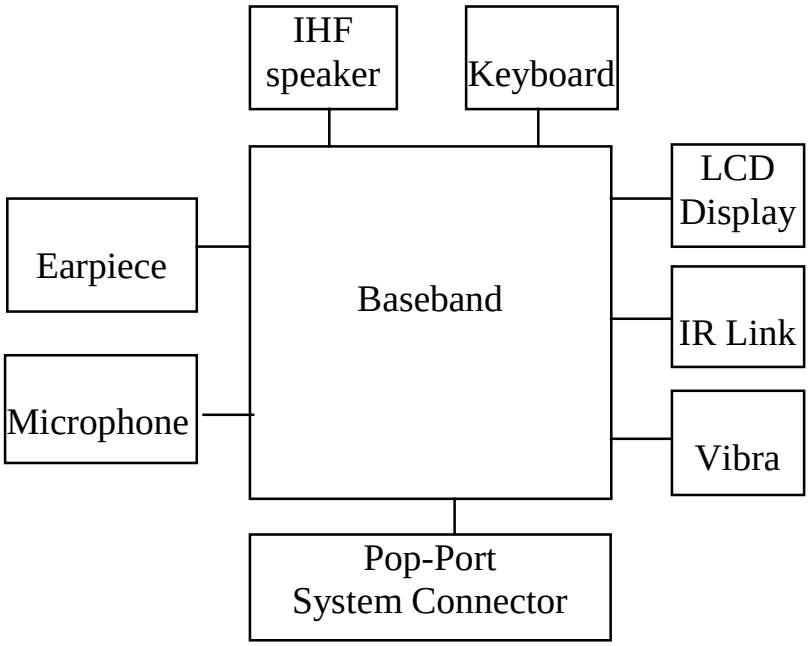
6. NHL-12 User Interface

The row and column lines of the UI are controlled by OMAP1510 and backlights by UEM.

Figure 7, “BB UI connections,” describes the BB user interface connections:

Figure 7:BB UI connections



S60 - LCD interface

The user interface features a 176x208 pixel active matrix colour TFT display with 65536 colours.

The backlight voltage is generated using a regulator (D4451). Figure 8, “Interface connections.,” shows the LCD interface connections:

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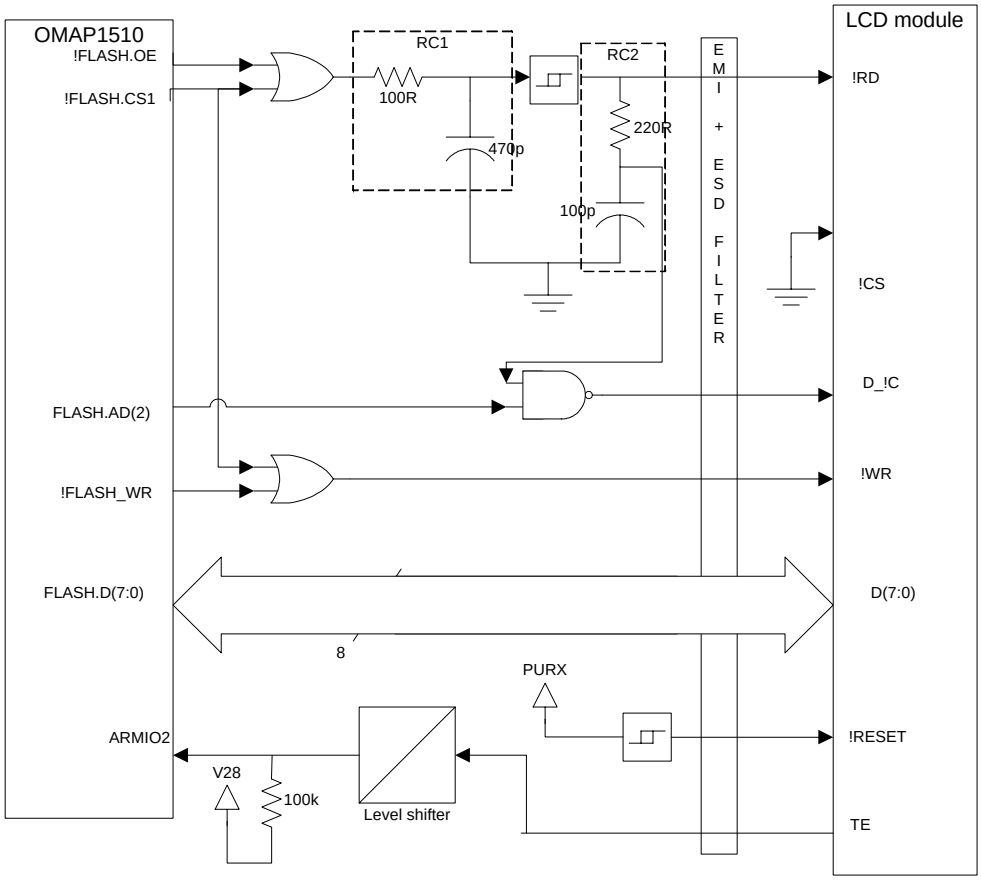
Figure 8:Interface connections.



The interface uses a 8-bit data transfer. Partial display function is implemented in the module.

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LCD & keypad illumination

In NHL-12, white LEDs are used for LCD lighting and blue for keypad lighting. There are four blue LEDs for keypad backlight. All LEDs have their own series resistors. A step-up DC-DC converter is used as a LED driver.

Table 14: DC characteristics and PIN assignments

Pin no.	Symbol	i/O	Description
1	GND	Ground	
2 3 4	IWR GND D0	Input Ground Bi-directional	Memory write enable (low active Data bus
5	D1	Bi-directional	Data bus
6	D2	Bi-directional	Data bus
7	D3	Bi-directional	Data bus
8	GND	Ground	
9 10 11	VDDI VDD LGND	Power supply Power supply Ground	Supply voltage for digital circuits Supply voltage for analogue circuits Guard ring ground for LEDs
12	LEDin	Power supply	LED anode
13	LEDout	Power supply	LED cathode
14	L_GND	Ground	Guard ring ground for LEDs
15	ICS	Input	Chip select (low active)
16 17 18	DAC GND D7	Input Ground Bi-directional	Data/command information signal Data bus
19	D6	Bi-directional	Data bus
20	D5	Bi-directional	Data bus
21	D4	Bi-directional	Data bus
22	TF	Output	Tearing effect
23 24	IRD IRES	Input Input	Memory read enable (low active) Reset signal (low active)

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Current consumption

Table 15: LCD interface current consumption

Display mode	Image	I_{VDD} (mA)		I_{VDDI} (mA)		Power (mW)
		Typ.	Max.	Typ.	Max.	Typ.
Normal	Typical (standard UI menu)	5.6	6.8	0.39	0.76	16.3
Normal	Worst case (B/W H-stripe)	7.3	8.9	0.40	0.73	21.1
Partial	Typical (208 lines UI menu)	3.1	3.6	0.29	0.45	9.0
Partial	Worst case (208 lines B/W H-stripe)	3.9	4.7	0.31	0.45	11.4
Partial	Worst case (40 lines B/W H-stripe)	1.3	1.6	0.20	0.42	4.1
Partial-idle	Worst case (40-lines, solid black)	0.49	0.70	0.16	0.40	1.7
Sleep	-	0.01	0.01	0.06	0.13	0.13

Maximum ratings

Table 16: LCD interface absolute maximum ratings

Parameter	Symbol	Min.	Max.	Unit
Supply voltage for digital circuits	VDDI	−0.5	+2.2	V
Supply voltage for analogue circuits	VDD	−0.1	+3.6	V
Signal input voltage	V_I	−0.3	VDDI+0.3	V
Signal output voltage	V_O	−0.3	VDDI+0.3	V
LED input current	I_{LED}	0	30	mA
LED power dissipation	P_{LED}	-	120	mW

Camera interface

NHL-12 features a built-in VGA camera.

The camera control interface operates by I2C bus.

The camera module itself is assembled into the metal frame and connected to the PWB via a 20-pin spring connector.

Camera powering voltages, V28&V18, are routed through the X4450 connector.

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Keyboard

The keyboard interface of OMAP1510 is a 6x5 matrix interface. The keyboard interface pins are normal IOs with 30/70 decision limits at 2,8 operating voltage: 1.96V high level and 0,84V low level.

Table 17: Key connection example

	Kbr(0)	Kbr(1)	Kbr(2)	Kbr(3)	Kbr(4)	Kbr(5)
Kbc(0)	Soft1	Soft2				
Kbc(1)	App/Averell					
Kbc(2)			Edit	1	4	7
Kbc(3)			*	2	5	8
Kbc(4)			#	3	6	9
Kbc(5)			Clear	0	Send	End

Table 18: Rocker connection

	ARMIO0	
ARMIO7	ARMIO4	ARMIO1
	ARMIO6	

Bluetooth

Bluetooth provides a fully digital link for communication between master unit and one or more slave units. The system provides a radio link that offers a high degree of flexibility to support various applications. Data and control interface for a low power RF module is provided. Data is regulated between the master and the slave.

The Bluetooth system in NHL-12 is compliant with the Bluetooth specification V1.1. The system is based on single chip Bluetooth solution, BC02. The chip contains radio and baseband parts as well as MCU and on-chip ROM memory. Together with some external components (matching components, filter, balun etc.) and an antenna, it forms the Bluetooth system, which can be attached to the host (OMAP1510). Bluetooth components are mounted directly to the PWB.

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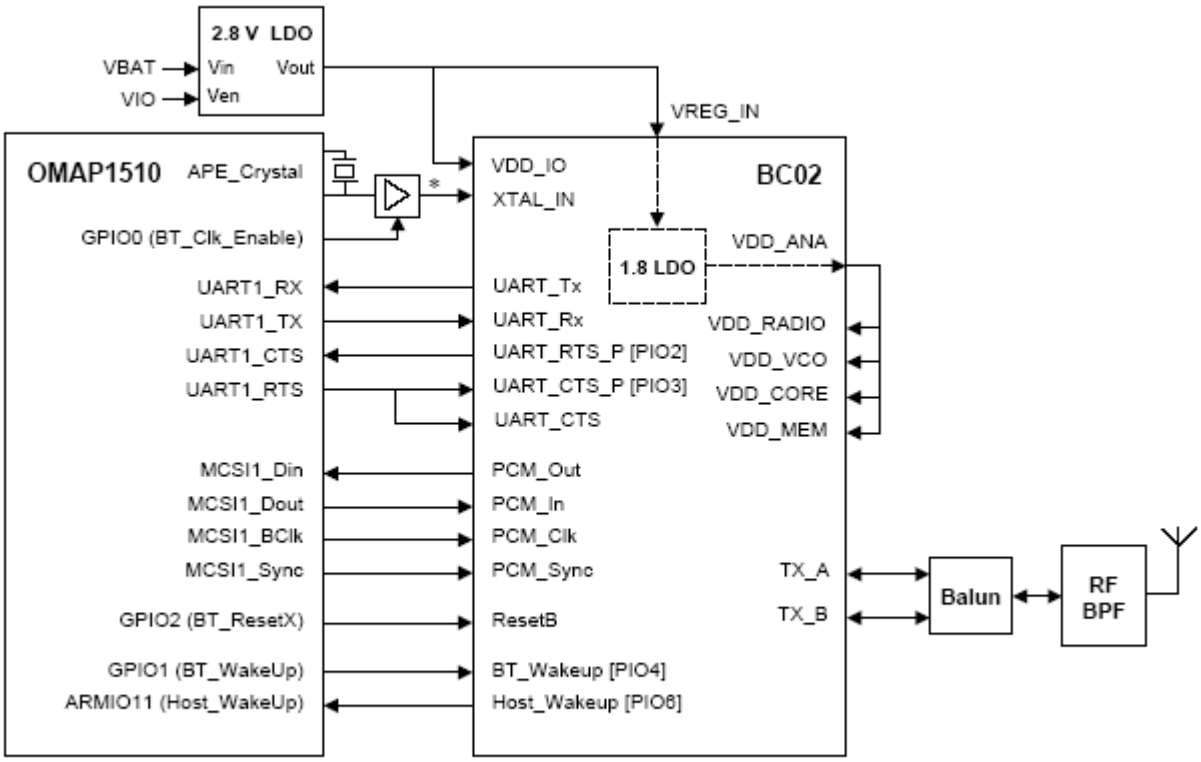
Figure 9:Bluetooth system



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7. SIM Interface

UEM contains the SIM interface logic level shifting. SIM interface supports 3V and 1.8V SIMs. SIM supply voltage is selected by a register in the UEM. It is only allowed to change the SIM supply voltage when the SIM IF is powered down.

The SIM interface is powered up when the SIMCardDet signal indicates "card in". This signal is derived from the BSI signal.

Table 19: SIM interface signals

Parameter	Variable	Min.	Typ	Max	Unit
SIMCARDet, BSI comparator Threshold	Vkey	1.94	2.1	2.26	V
SIMCARDet, BSI comparator Hysteresis (1)	Vsimhyst	50	75	100	mV

The entire SIM interface is located in two chips: UPP and UEM.

The SIM interface in the UEM contains:

- power up/down
- port gating
- card detect
- data receiving
- ATR-counter
- registers
- level shifting buffers logic

The SIM interface is the electrical interface between the SIM card and the mobile phone (via UEM device).

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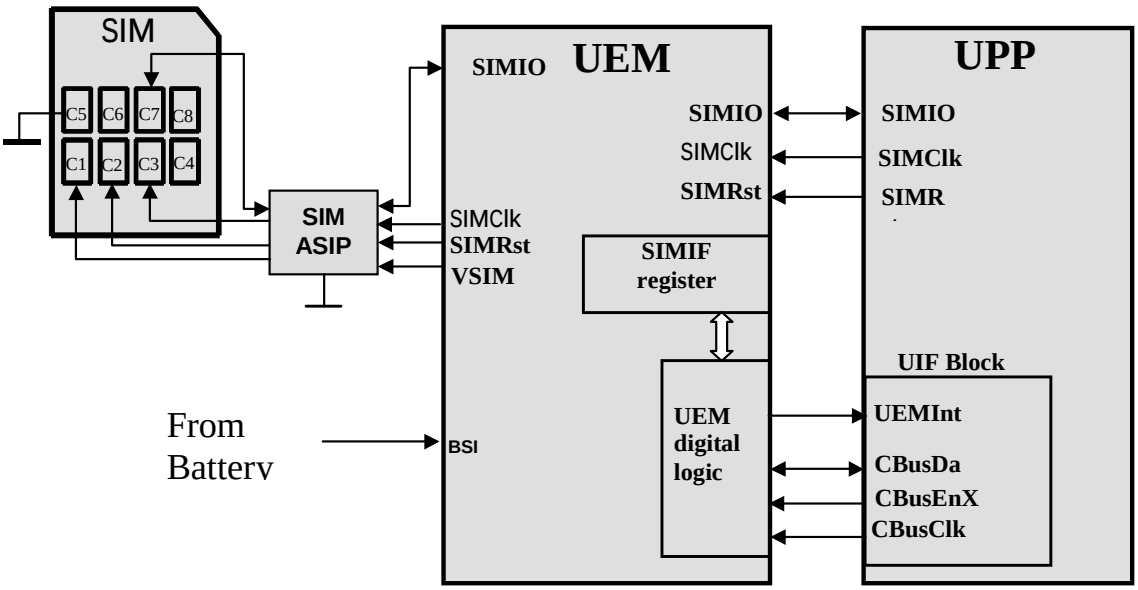
Figure 10:SIM interface NHL-12



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8. System Connector Interface

The system connector in NHL-12 is a Pop-Port™ connector. It consists of a charging plug socket and system connector. The Pop-Port is a feature-based interface. The accessory contains information about its features (ACI ASIC) and it is detected with a fully digital detection procedure.

Four new functions are introduced with the Pop-Port™ system connector interface:

- Accessory control interface (ACI)
- Power out
- Stereo audio output
- Universal serial bus (USB)

Table 20: Pop-port™ functions

Function	Note
Charging	Pads for 2-wire charging in cradles
Audio	4-wire fully differential stereo audio output
Power supply for accessories	2.78V/70mA output to accessories
ACI (Accessory Control Interface)	Accessory detection/removal & controlling
FBUS	Standard FBUS, Fast FBUS *Note! NHL-12 does not support accessories using FBUS serial interface.*
USB (default)	USB v.2.0 device mode (full speed 12M)

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Figure 11:Pop-Port™ connections

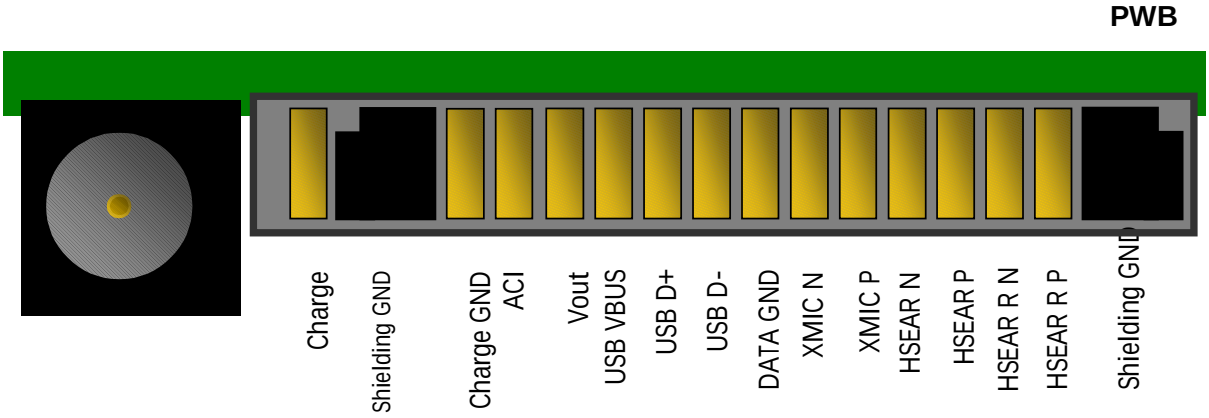

Table 21: Pop-port™ connections

Pin #	Signal	Note
1	VCHAR	
2	GND	Charge ground
3	ACI	Insertion & removal detection /Serial data bi-directional 1 kbit/s
4	Vout	200mW
5	USB VBUS	
6	USB D+/FBUS Rx	
7	USB D-/FBUS Tx	
8	USB data GND	Data ground
9	XMIC N	Negative audio in signal
10	XMIC P	Positive audio in signal
11	HSEAR N	Negative audio out signal. Max bandwidth from the phone
12	HSEAR P	Positive audio out signal. Max bandwidth from the phone
13	HSEAR R N	Not connected or grounded in mono.
14	HSEAR R P	Not connected or grounded in mono.

Universal Serial Bus (USB)

The USB interface of OMAP1510 supports the implementation of a full speed device, fully compliant to USB2.0 standard. NHL-12 uses an integrated USB transceiver.

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OMAP1510 can provide a maximum of three sets of USB ports. One set is an integrated USB transceiver and the other two sets are LVCMOS I/O pins that implement interfaces to external transceivers. However, only the first set is available by default and used in the NHL-12 engine.

Accessory Control Interface (ACI)

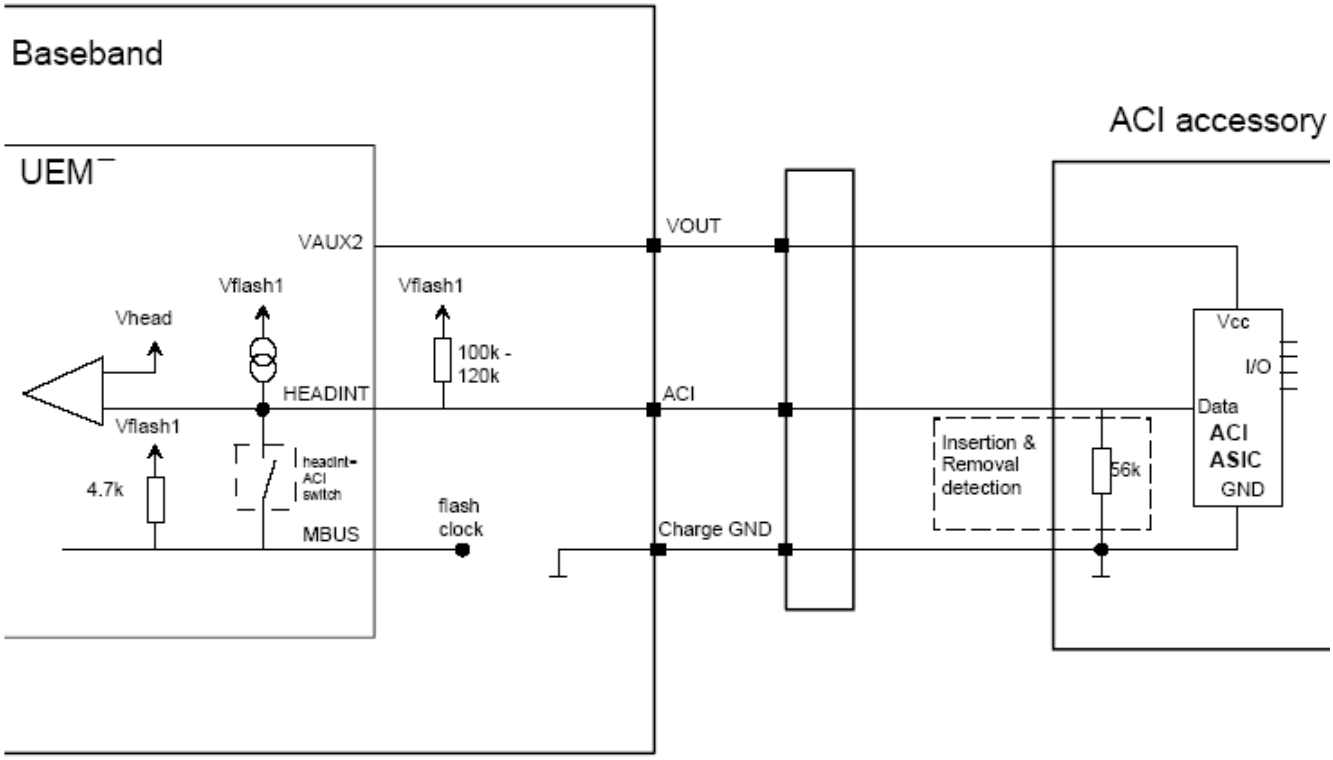
ACI (Accessory Control Interface) is a point-to-point, bi-directional serial bus. ACI has two main features: 1) detecting the insertion and/or removal of an accessory device and 2) acting as a data bus.

Third feature provided by ACI is to identify and authenticate a specific accessory which is connected to the system connector interface.

All accessories cause *headint* interrupt when connected to or disconnected from the system connector. The insertion of an accessory generates a headint interrupt by pulling the ACI line down. When no accessory is present, the UEM's internal headint pull-up resistor keeps the line high.

All accessories have a common detection start sequence, when phone gets headint interrupt from high to low transition in the ACI pin.

Figure 12:Principle schematics of ACI accessory and engine



VOUT (Accessory Voltage Regulator)

An external LDO Regulator is needed for accessory power supply purposes. All ACI accessories require this power supply. Regulator input is connected to the battery voltage VBAT and output is connected to the Vout pin. The regulator is controlled via UPP (On/Off-function).

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Figure 13:Accessory power supply diagram

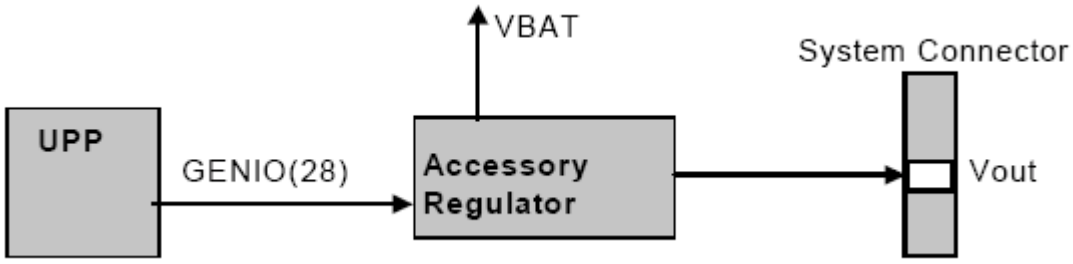

Table 22: Accessory power supplies

Signal	Min	Nom	Max	Note
Vout	2.70V	2.78	2.86V	I_{max} = 150mA
GenIO(28)	1.4	1.8	1.88 0.6	High (ON) Low (OFF)

HookInt

The *hookInt* signal is generated by creating a short circuit between the headset microphone signals. An LP filter is needed on the hookInt input to filter the audio signal. In this mode, the earpiece signal on the HF and HFCM pins is in the opposite phase. The earpiece is driven differentially.

When no accessory is present, the hookInt signal is pulled up with the UEM resistor. When the accessory is inserted and the microphone path is biased, the hookInt signal decreases to 1.8V due to the microphone bias current flowing through the resistor. When the microphone button is pressed, the microphone signals are connected together, and the hookInt input will get half of micbias dc value 1.1 V. This change in DC level causes the hookInt comparator output to change state, in this case from 0 to 1. The button can be used for answering incoming calls but not to initiate outgoing calls.

Table 23: HookInt signals

Signal	Min	Nom	Max	Unit
VFLASH1	2.7	2.78	2.86	V
MICB2	2.0	2.1	2.25 600	V uA
Vhook1	1.25	1.35	1.45	V

Charging

NHL-12 can be charged via a DC-plug or charging pins on the system connector. Only 2-wire charging is supported.

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DC-plug

NHL-12 uses a 3.5mm DC-plug. 3-wire chargers are supported, but 3-wire charging is not. In practice this means that the 3-wire chargers are internally connected (charger control wire connected to GND) as 2-wire chargers. 1Hz PWM signal is used to control UEM's charge switch.

VCHAR pins of system connector

The VCHAR and ChargeGND pin are directly connected to the normal charger lines of the DC-plug.

Table 24: VCHAR pins of system connector

Signal	Min	Nom	Max	Unit	Note
Input voltage range (fast charger)	5.5	8.4	9.3	VRMS	I= 850mA
Input voltage range (standard charger)		11.1 7.9	16	Vpeak VRMS	
	-0.3		20	V	Absolute maximum VHAR voltage

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9. Baseband Serial Interfaces

Internal serial interfaces between CMT and APE

XBUS

XBUS is the main communication interface between the CMT and APE engines. This 6-pin interface is a combination of a general 4-pin UART based interface and two wake-up signals. XBUS has no test points and the signals are routed in the inner layers of the PWB.

XABUS

XABUS is a synchronous serial interface used for uncompressed PCM audio data transfer between the DSPs of UPP (CMT) and OMAP1510 (APE).

External serial interfaces

MMC interface

The MMC interface consists of a control block in OMAP1510, MMC regulator and EMC protection ASIP (R5200). MMC interface is a serial bus with three wires: data, command and clock run at 16MHz. The regulator (N5200) output is VMMC.

IrDA interface

NHL-12 uses a TDFU5103 IR-module (V4451). It is compatible with 1.152Mbit IrDA 1.3. Speeds up to 115kbits/sec are supported. Operating voltages are VBAT and V28.

USB interface

Pop-Port™ system connector has pins for USB interface, for a USB 2.0 full speed (12Mb/s) compliant access. The interface consists of a USB regulator (N2001) supplying V33 to OMAP1510 USB control block, and USB ASIP (R2003) for EMC protection.

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10. Baseband Test Points

List and description

Table 25: Baseband test points

Test point	Signal	Function	Characteristics	Note
J2400	MCSI2_DIN	XABUS receive data	1.8V digital signal	Data to OMAP1510 from UPP
J2401	MCSI2_DOUT	XABUS transmit data	1.8V digital signal	Data from OMAP1510 to UPP
J2402	MCSI2_SYNC	XABUS synchronization	8 kHz digital clock 1.8V	Sync clock from UPP to OMAP1510
J2404	COM_MCLK_REQ	XABUS clock request	1.8V digital signal	Clock request to OMAP1510 from UPP
J2405	MCSI2_CLK	XABUS clock	12 MHz digital clock 1.8V	Clock from OMAP1510
N4800#3	PURX	Power_up reset	1.8V digital signal	From UEM to UPP
J2801	SLEEPX	Sleep mode control signal	1.8V when not in sleep mode	From UPP to UEM
			0 V when in sleep mode	
J2802	SLEEPClk	Sleep mode timing clock	32.768kHz digital clock 1.8V	From UEM to UPP;
J2803	UEMINT	Interrupt request from UPP	1.8V digital signal	From UEM to UPP
J4815	CLK32k	sleep mode clock	32.768kHz digital clock 1.8V	From UEM to OMAP1510
J2807	MBUSTX	MBUS from UPP to UEM	1.8V digital signal	
J2808	MBUSRX	MBUS from UEM to UPP	1.8V digital signal	
J2809	FBUSTX	FBUS from UPP to UEM	1.8V digital signal	
J2810	FBUSRX	FBUS from UEM to UPP	1.8V digital signal	

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Table 25: Baseband test points

Test point	Signal	Function	Characteristics	Note
J2811	DBUSClk	Dbus clock	13MHz digital clock signal 1.8V	From UPP (DSP) to UEM
				Generated by UPP
J2813	DBUSEN1X	UPP	1.8V digital signal	From UPP (DSP) to UEM
J2815	EXTRDX	Flash memory write enable	1.8V digital signal	
J2817	FLSCLK	Flash memory clock	3.5MHz digital clock signal 1.8V	In burst mode
J2818	FLSCSX	Flash memory chip select	1.8V digital signal	
J4100	DIN	I2S format serial data input	2.8V digital signal	from OMAP1510 to stereo DAC
J4801	NFWE	Flash write enable	1.8V digital signal	From omap1510 to NAND flash
J4802	NFOE	flash output enable	1.8V digital signal	From omap1510 to NAND flash
J4803	NFRP	flash reset/ power down	1.8V digital signal	From omap1510 to NAND flash
J4804	NFADV	address valid strobe	1.8V digital signal	From omap1510 to NAND flash
J4805	NFCSO	flash chip select	1.8V digital signal	From omap1510 to NAND flash
J4806	FCLK	flash clock	37.5MHz(typ.) digital clock 1.8V	From omap1510 to NAND flash
J4807	FDATA	flash data bus	1.8V digital signal	from/to OMAP1510 to/from NAND flash
R4802	MPU_nRESET	power on/reset		from UPP/UEM to OMAP1510
J4810	NSRAS	SDRAM row address strobe	1.8V digital signal	from OMAP1510 to SDRAM
J4811	NSCAS	SDRAM col-umn address strobe	1.8V digital signal	from OMAP1510 to SDRAM

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Table 25: Baseband test points

Test point	Signal	Function	Characteristics	Note
J4812	NSWE	SDRAM write enable	1.8V digital signal	from OMAP1510 to SDRAM
J4813	SDCLK_EN	SDRAM clock enable	1.8V digital signal	from OMAP1510 to SDRAM
J4814	SDATA	SDRAM data bus	1.8V digital signal	from/to OMAP1510 to/from SDRAM
J5000	INT	Seija flash interface interrupt signal	max. 0.2V digital signal	from seija interface to OMAP1510
R4808	SDCLK	SDRAM clock	72 MHz (typ.) digital clock 1.8V	from OMAP1510 to SDRAM
R2902	RFclk	system clock for baseband	26 MHz analog clock signal >300mVpp	from Helgo to UPP
J2020	VBATT	battery voltage		
J2021	BSI	Battery size indicator; flash programming start signal	1V in normal mode	To UEM A/D converter
			0V in local mode	
			If bsi line rises > 2.1V	
			2.78 BSI pulse	
J2022	GND	Ground		
J2031	VBATT	zocus IC calibration point	3.0 mOhm PWB trace	
J2032	VBAT	zocus IC calibration point	3.0 mOhm PWB trace	
J4450	TXD	transmit data	2.78V digital signal	from OMAP1510 to irda
J4451	RXD	receive data	2.78V digital signal	from Irda to OMAP1510
J4452	SD	shutdown	2.78V digital signal	from OMAP1510 to irda

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Table 25: Baseband test points

Test point	Signal	Function	Characteristics	Note
PRODTP1	FBUS_TX	Flash programming data and phone control	2.78V digital signal	From phone to FPS-8
PRODTP2	FBUS_RX	Flash programming data and phone control	2.78V digital signal	From FPS-8 to phone
PRODTP3	GND	Ground		
PRODTP4	USB_D+	USB data	full speed 12M, voltage range 0V-3.3V	bi-directional data between OMAP1510 and USB
PRODTP5	MBUS	Flash programming data and phone control	2.78 digital signal 6.5MHz max.	Bi-directional phone control
PRODTP6	VPP	Flash programming voltage	1.8V internal voltage or 12 V external voltage	
PRODTP7	GND	Ground		
PRODTP8	USB_5V	USB Vbus, DC in	4.375V -5.25V voltage range	to OMAP1510
PRODTP9	USB_D-	USB data	full speed 12M, voltage range 0V-3.3V	bi-directional data between OMAP1510 and USB

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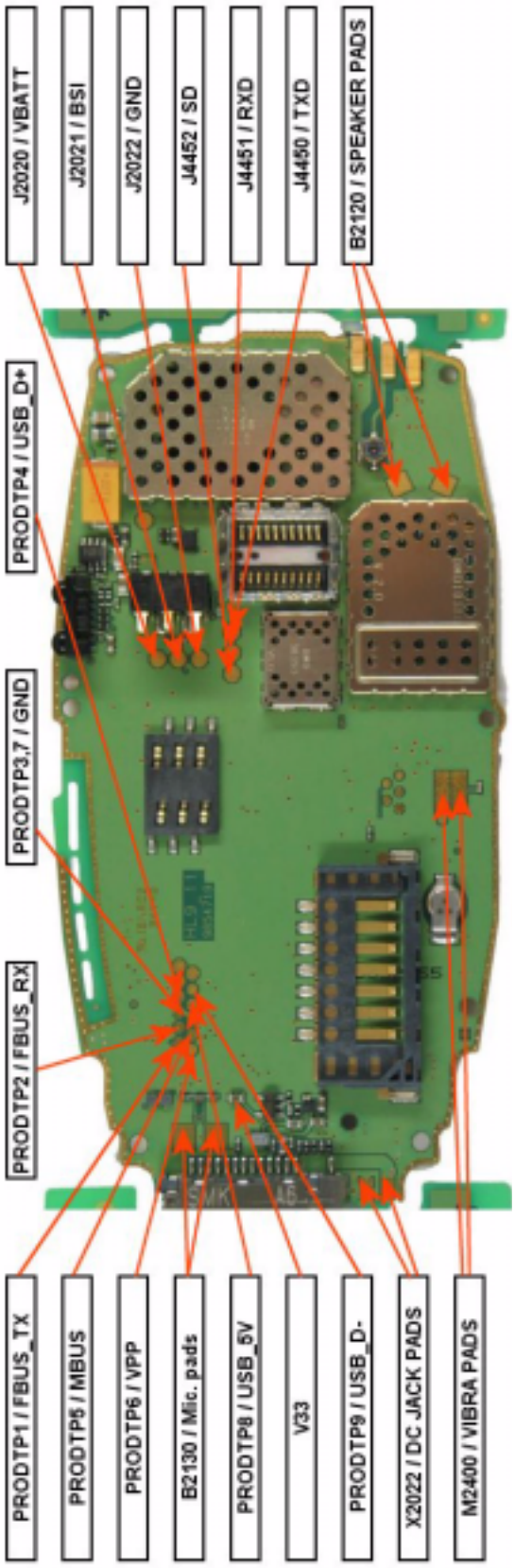
Test points on bottom-side



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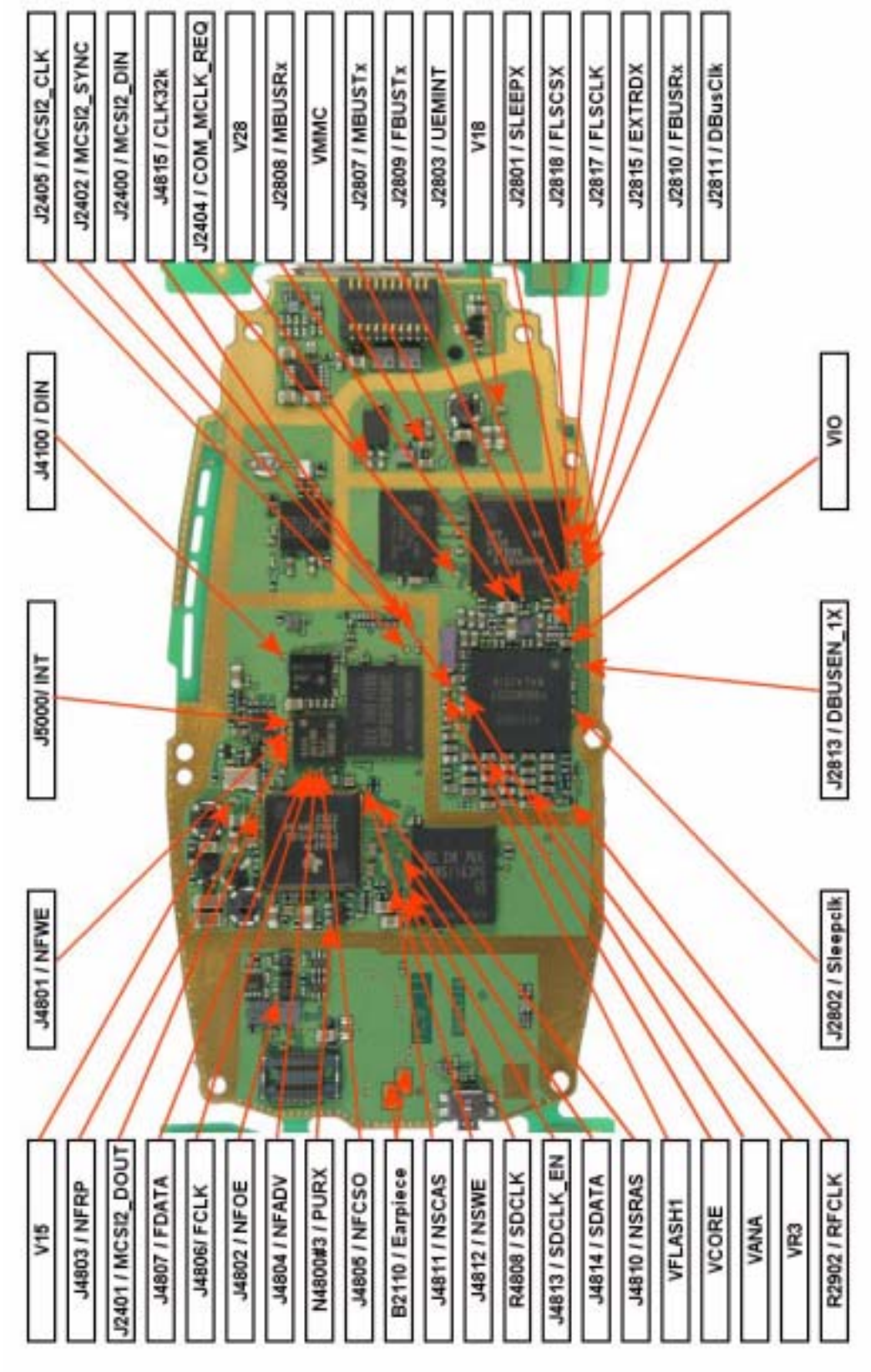
Test points on top-side



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11. Baseband Troubleshooting

This section is a guide for localizing and repairing electrical faults in NHL-12 baseband.

Before any service operation you must be familiar with the NHL-12 product and module level architecture. You have to be also familiar with the NHL-12 specific service tools such as the Phoenix service software and flashing tools.

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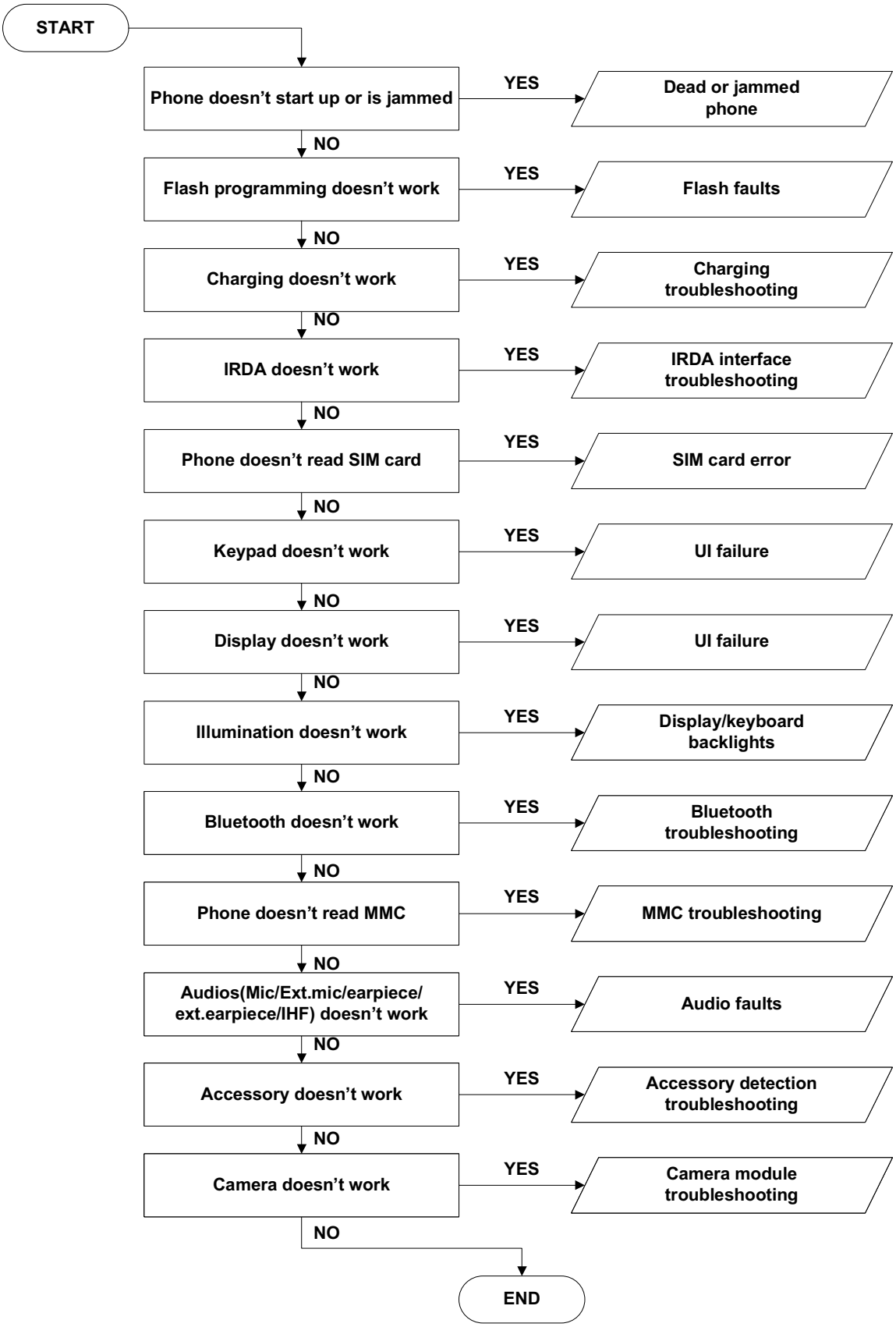
Top level flowchart



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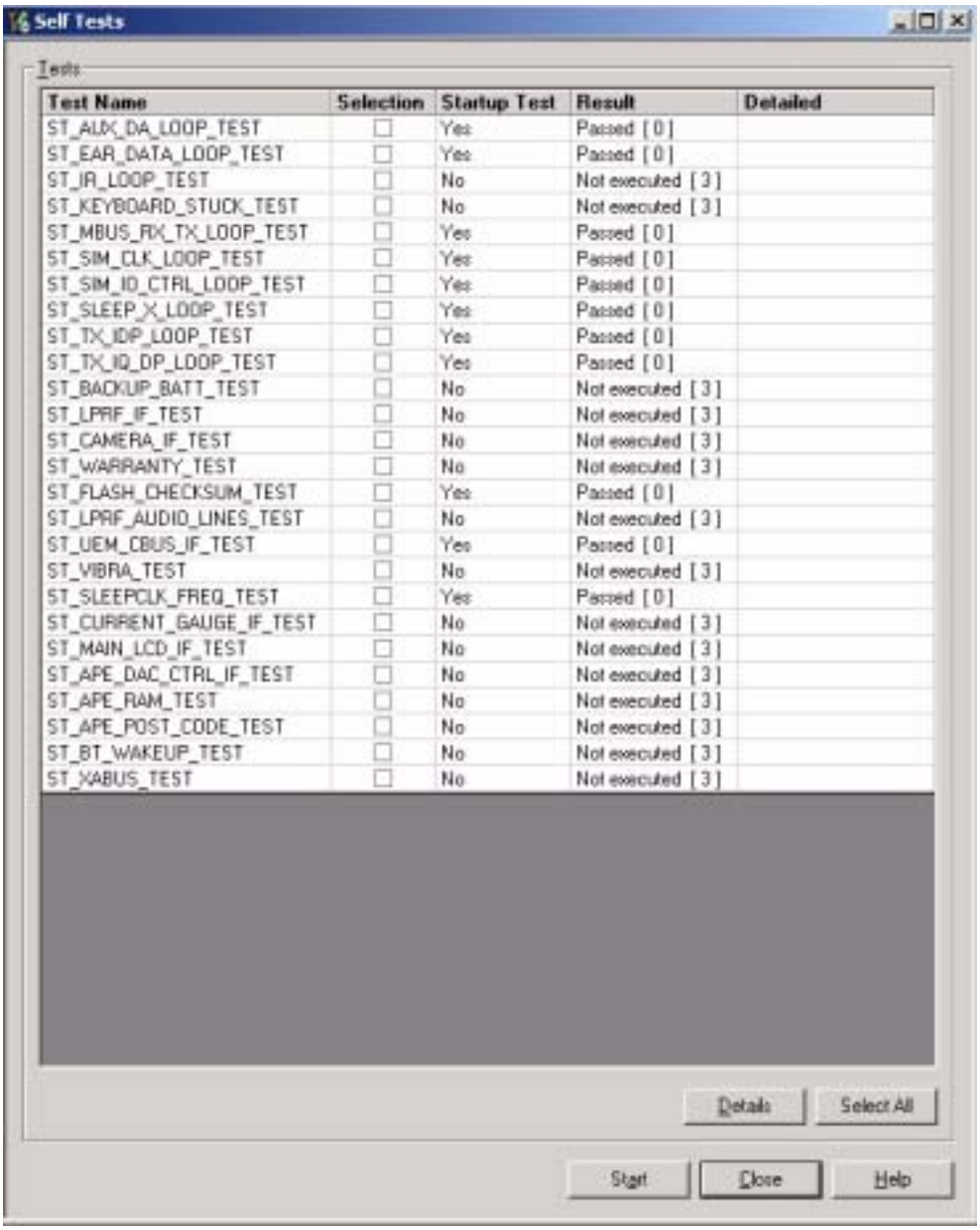
“Contact Service” on display

When the phone is powered on, self-test functions are executed and if one or more self-test functions fails, the message “Contact Service” is shown on the display.

This fault means that the phone software is able to run and thus the watchdog of UEM can be served.

MCU self-test cases can be split into two categories: the ones that are executed during power up and the ones that are executed only with a PC connected. These tests and the items included are as follows:

Figure 14:MCU self-tests



If some self-test failed, kindly refer to the relevant chapter in this troubleshooting document.

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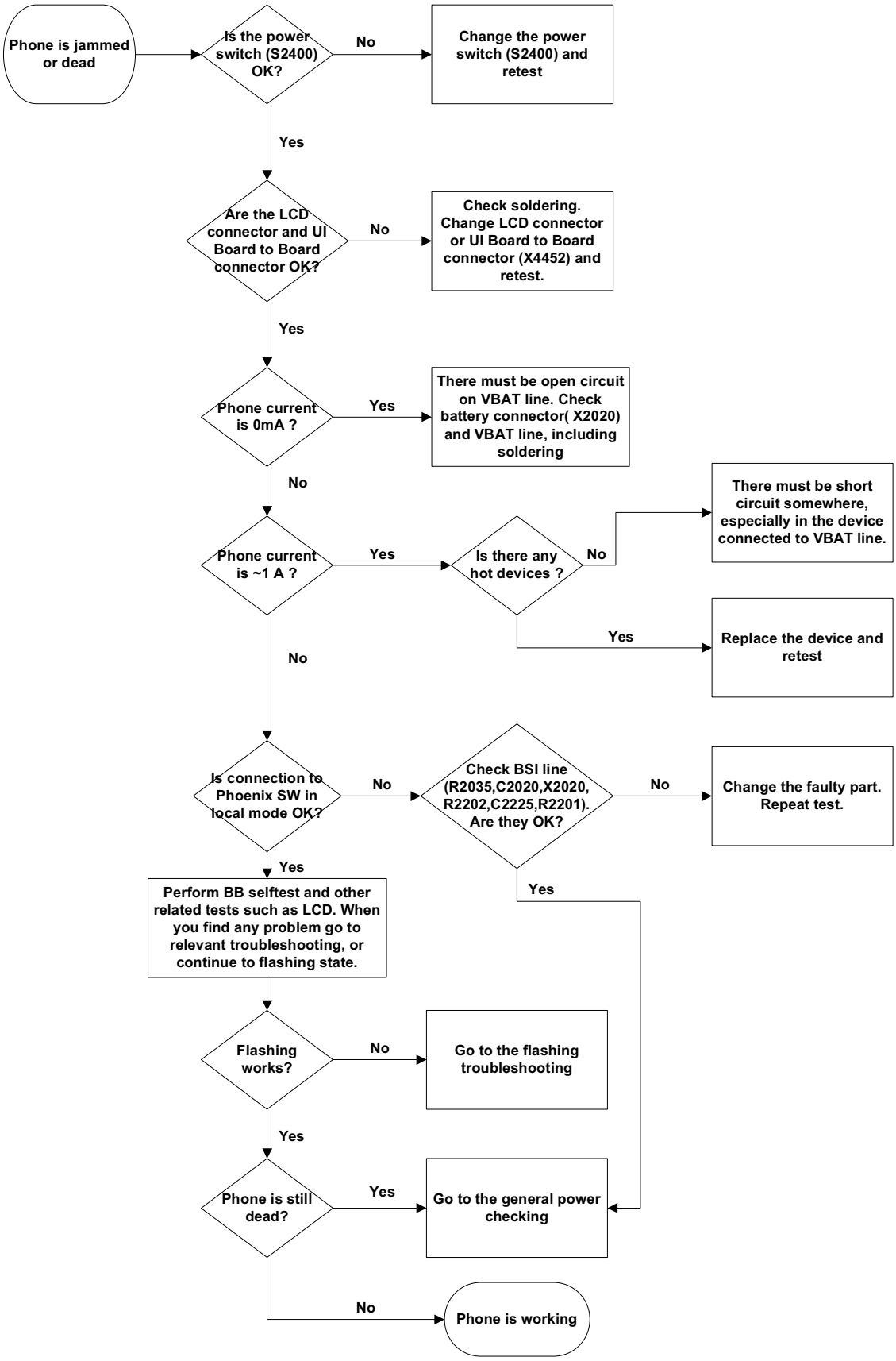
Dead or jammed phone


Phone is jammed or dead
Is the power switch (S2400) OK?
No
Change the power switch (S2400) and retest
Yes
Are the LCD connector and UI Board to Board connector OK?
No
Check soldering. Change LCD connector or UI Board to Board connector (X4452) and retest.
Yes
Phone current is 0mA ?
Yes
There must be open circuit on VBAT line. Check battery connector(X2020) and VBAT line, including soldering
No
Phone current is ~1 A ?
Yes
Is there any hot devices ?
No
There must be short circuit somewhere, especially in the device connected to VBAT line.
Yes
Replace the device and retest
No
Is connection to Phoenix SW in local mode OK?
No
Check BSI line (R2035,C2020,X2020, R2202,C2225,R2201). Are they OK?
No
Change the faulty part. Repeat test.
Yes
Yes
Perform BB selftest and other related tests such as LCD. When you find any problem go to relevant troubleshooting, or continue to flashing state.
Flashing works?
No
Go to the flashing troubleshooting
Yes
Phone is still dead?
Yes
Go to the general power checking
No
Phone is working

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Flash faults

NHL-12 has three memory components installed on the main PWB. SDRAM and NAND components are interfaced with OMAP1510, while CMT flash is interfaced with the UPP8M ASIC.

You can flash the phone to find which one is causing problems. The necessary steps are described below. Phoenix error messages displayed during the flashing process help on defining what is wrong. To be able to flash the device, the majority of device BB area components must function properly.

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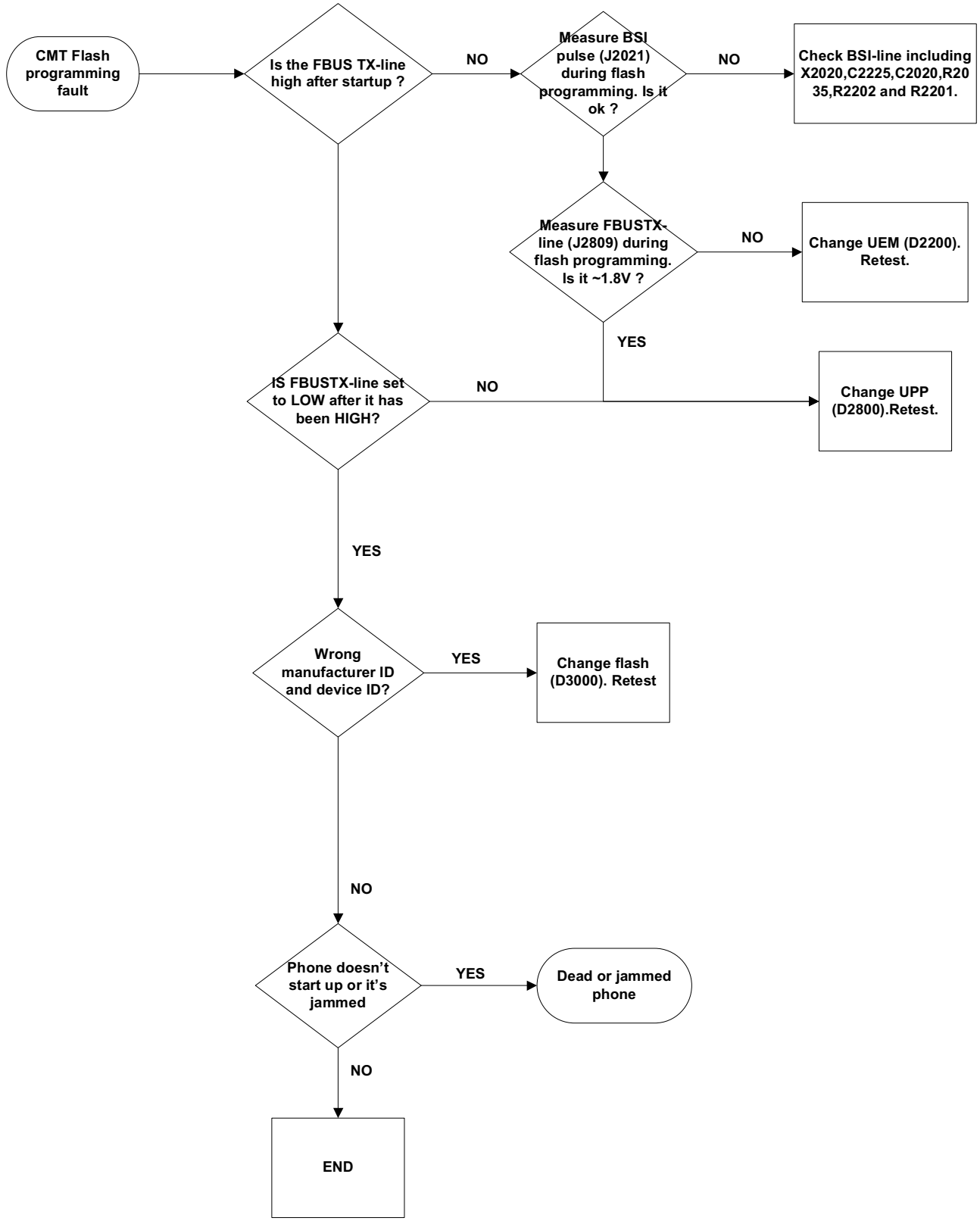
CMT flash faults



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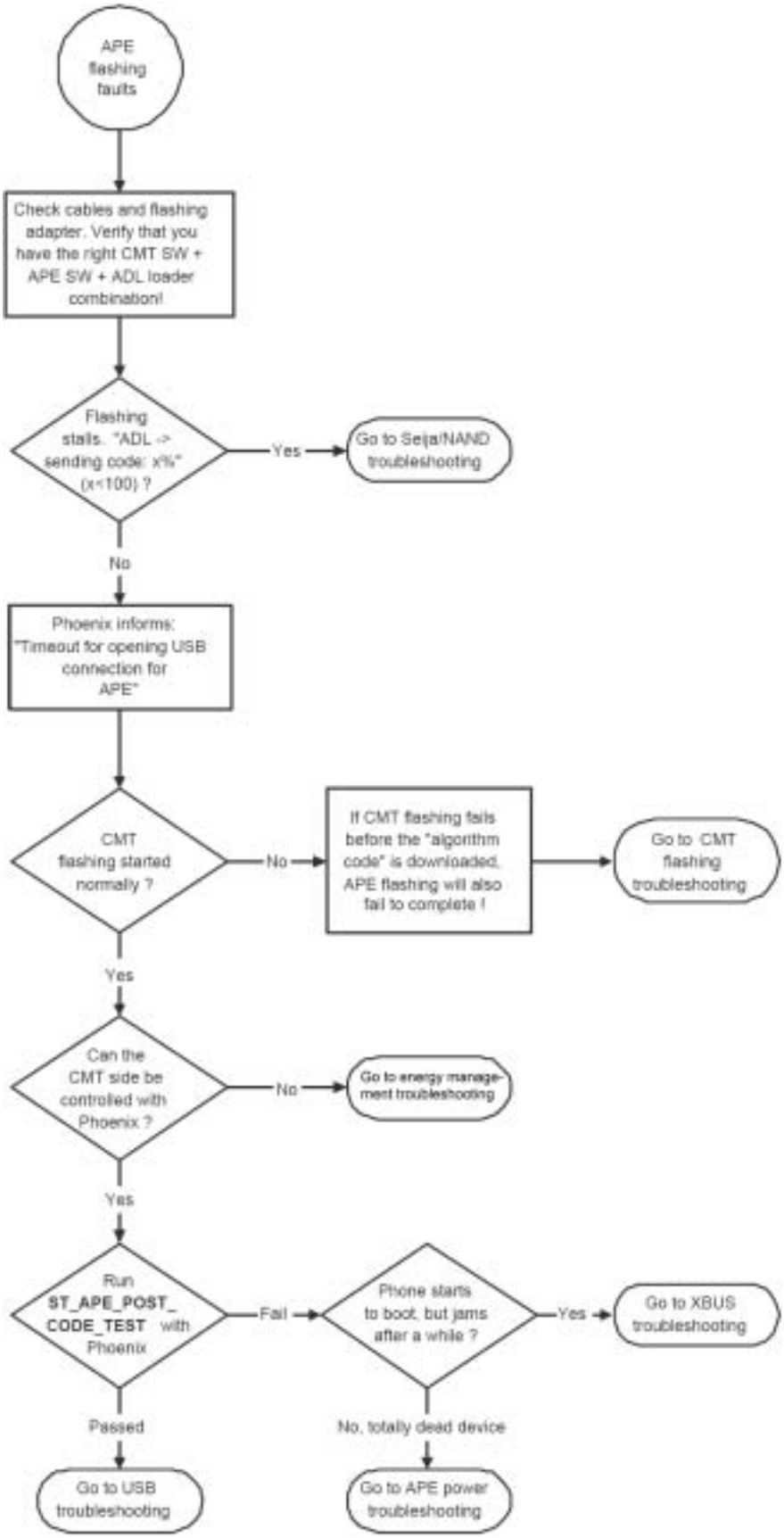
APE flash faults


APE flashing faults
Check cables and flashing adapter. Verify that you have the right CMT SW + APE SW + ADL loader combination!
Flashing stalls. "ADL -> sending code: x%" (x<100) ?
Yes
Go to Sejja/NAND troubleshooting
No
Phoenix informs: "Timeout for opening USB connection for APE"
CMT flashing started normally ?
No
If CMT flashing fails before the "algorithm code" is downloaded, APE flashing will also fail to complete !
Go to CMT flashing troubleshooting
Yes
Can the CMT side be controlled with Phoenix ?
No
Go to energy management troubleshooting
Yes
Run ST_APE_POST_CODE_TEST with Phoenix
Fail
Phone starts to boot, but jams after a while ?
Yes
Go to XBUS troubleshooting
Passed
No, totally dead device
Go to USB troubleshooting
Go to APE power troubleshooting

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APE memory troubleshooting

OMAP1510 flash (Seija)

Figure 15:OMAP1510 flash (Seija) (1/2)

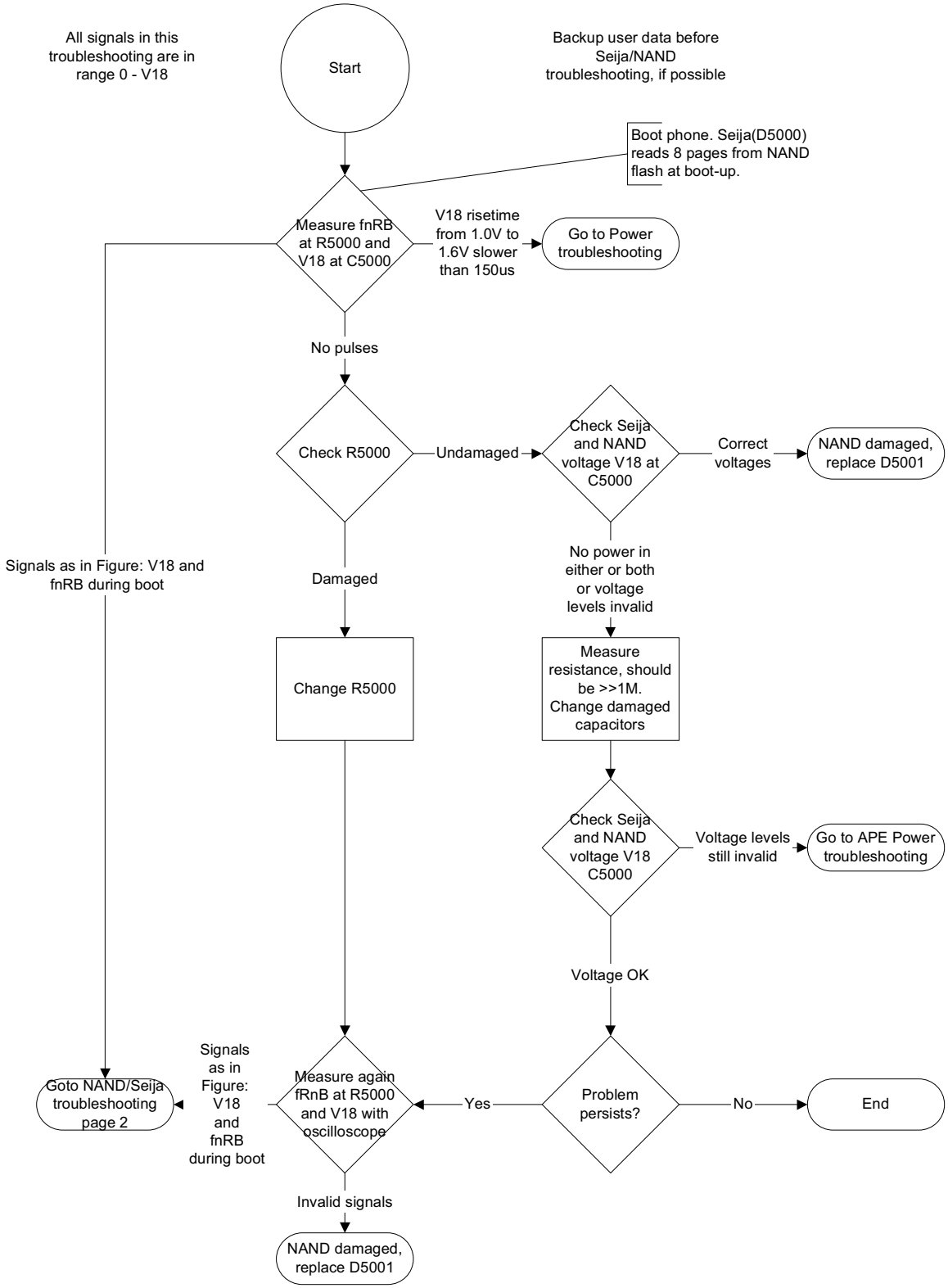
All signals in this troubleshooting are in range 0 - V18
Start
Backup user data before Seija/NAND troubleshooting, if possible
Boot phone. Seija(D5000) reads 8 pages from NAND flash at boot-up.
Measure fnRB at R5000 and V18 at C5000
V18 risetime from 1.0V to 1.6V slower than 150us
Go to Power troubleshooting
No pulses
Check R5000
Undamaged
Check Seija and NAND voltage V18 at C5000
Correct voltages
NAND damaged, replace D5001
Signals as in Figure: V18 and fnRB during boot
Damaged
No power in either or both or voltage levels invalid
Change R5000
Measure resistance, should be >>1M. Change damaged capacitors
Check Seija and NAND voltage V18 C5000
Voltage levels still invalid
Go to APE Power troubleshooting
Voltage OK
Goto NAND/Seija troubleshooting page 2
Signals as in Figure: V18 and fnRB during boot
Measure again fRnB at R5000 and V18 with oscilloscope
Yes
Problem persists?
No
End
Invalid signals
NAND damaged, replace D5001

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Figure 16:OMAP1510 flash (Seija) (2/2)

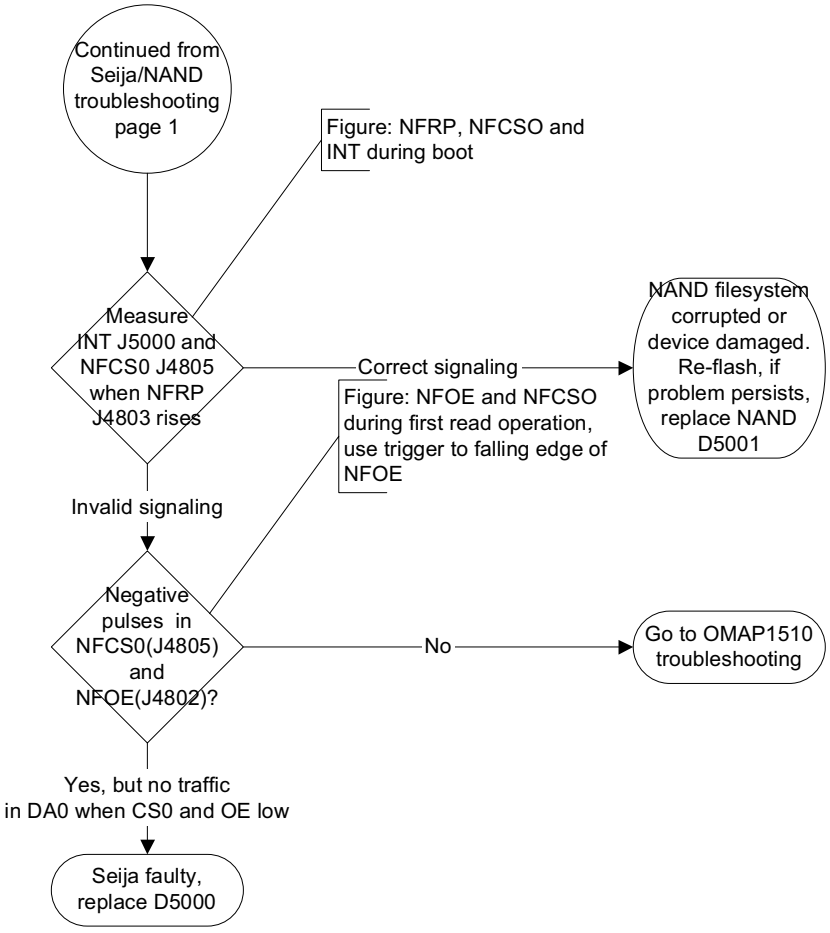
Continued from Seija/NAND troubleshooting page 1
Figure: NFRP, NFCSO and INT during boot
Measure INT J5000 and NFCS0 J4805 when NFRP J4803 rises
Correct signaling
NAND filesystem corrupted or device damaged. Re-flash, if problem persists, replace NAND D5001
Figure: NFOE and NFCSO during first read operation, use trigger to falling edge of NFOE
Invalid signaling
Negative pulses in NFCS0(J4805) and NFOE(J4802)?
No
Go to OMAP1510 troubleshooting
Yes, but no traffic in DA0 when CS0 and OE low
Seija faulty, replace D5000

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Figure 17:V18 and fnRB during boot

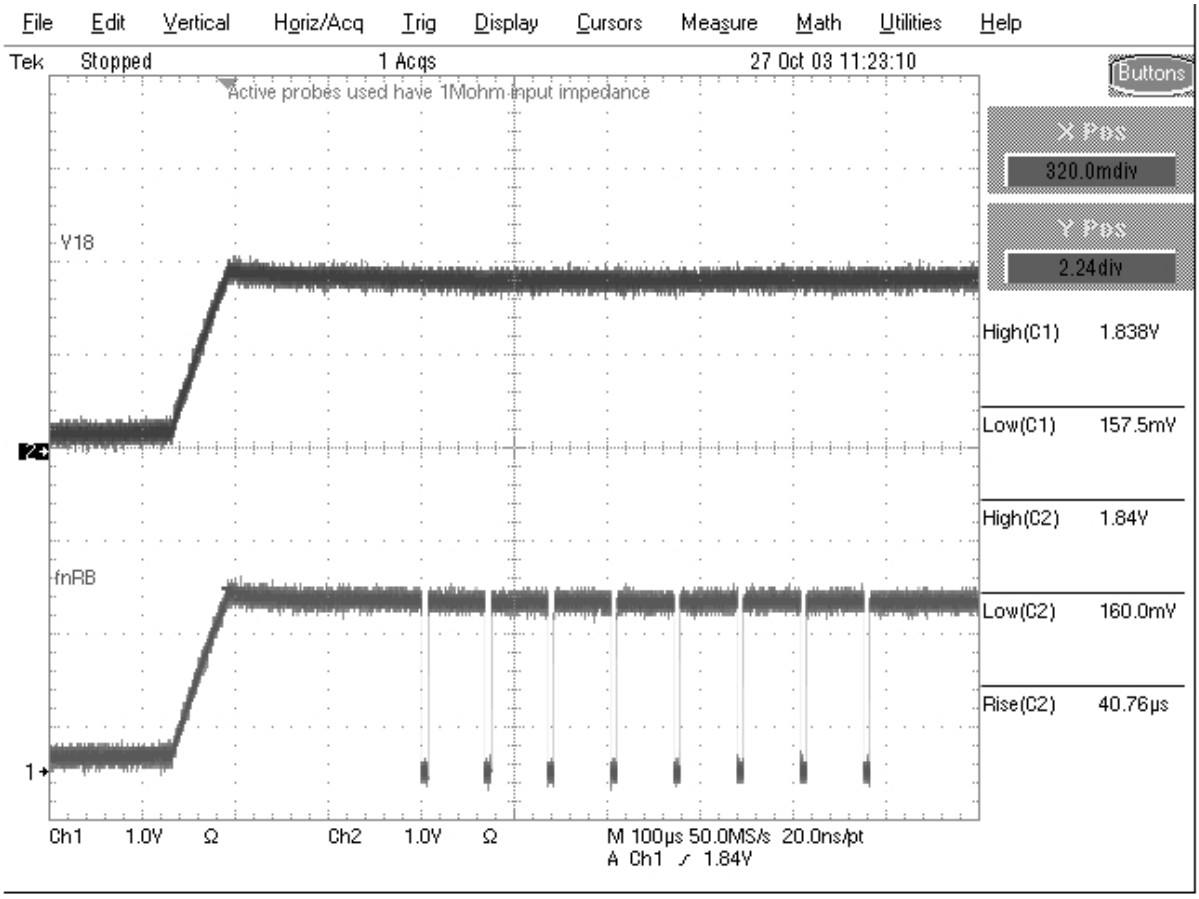

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Figure 18:NFRP, NFCSO and INT during boot

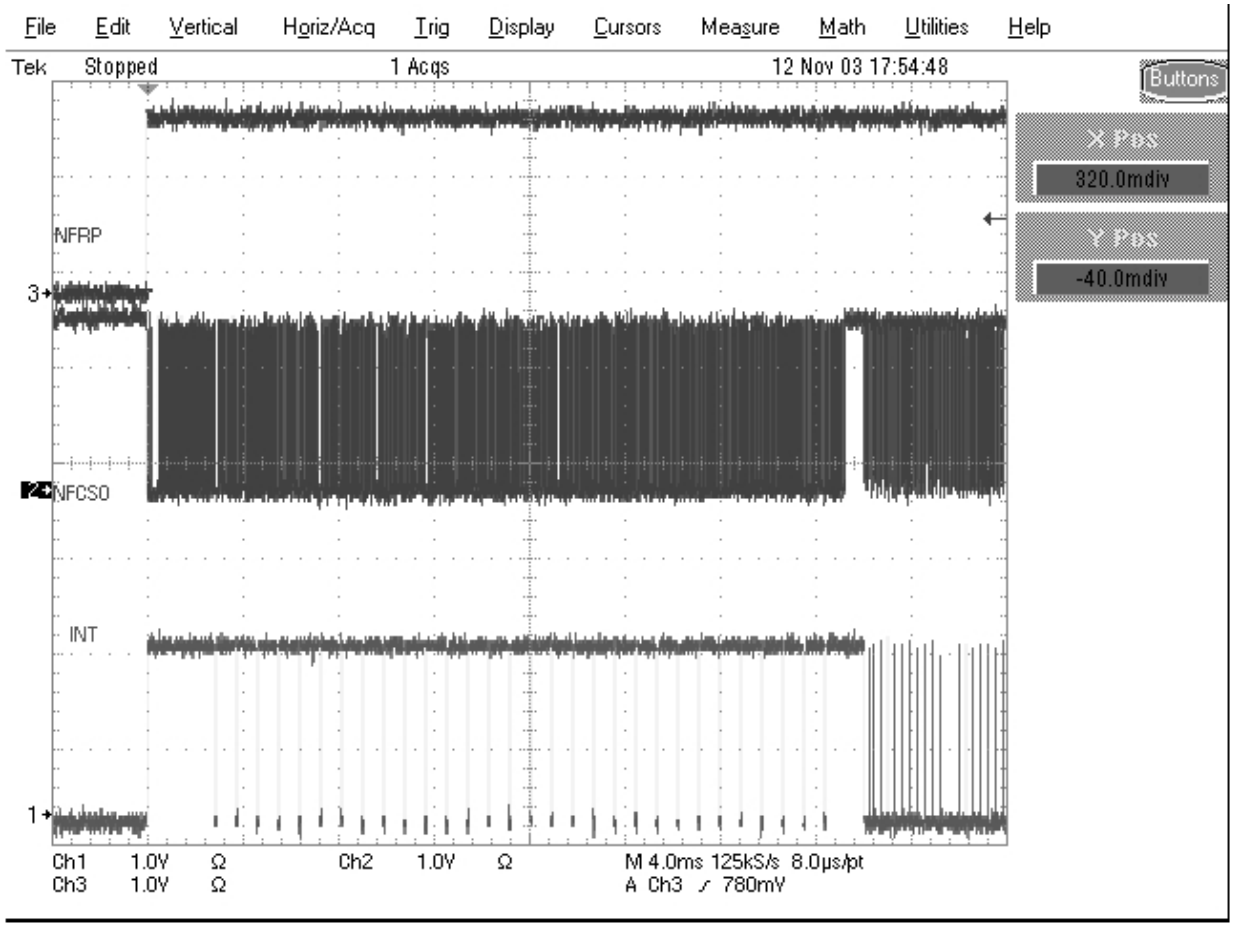

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Figure 19:NFOE and NFCSO during first read operation, use trigger to falling edge of NFOE

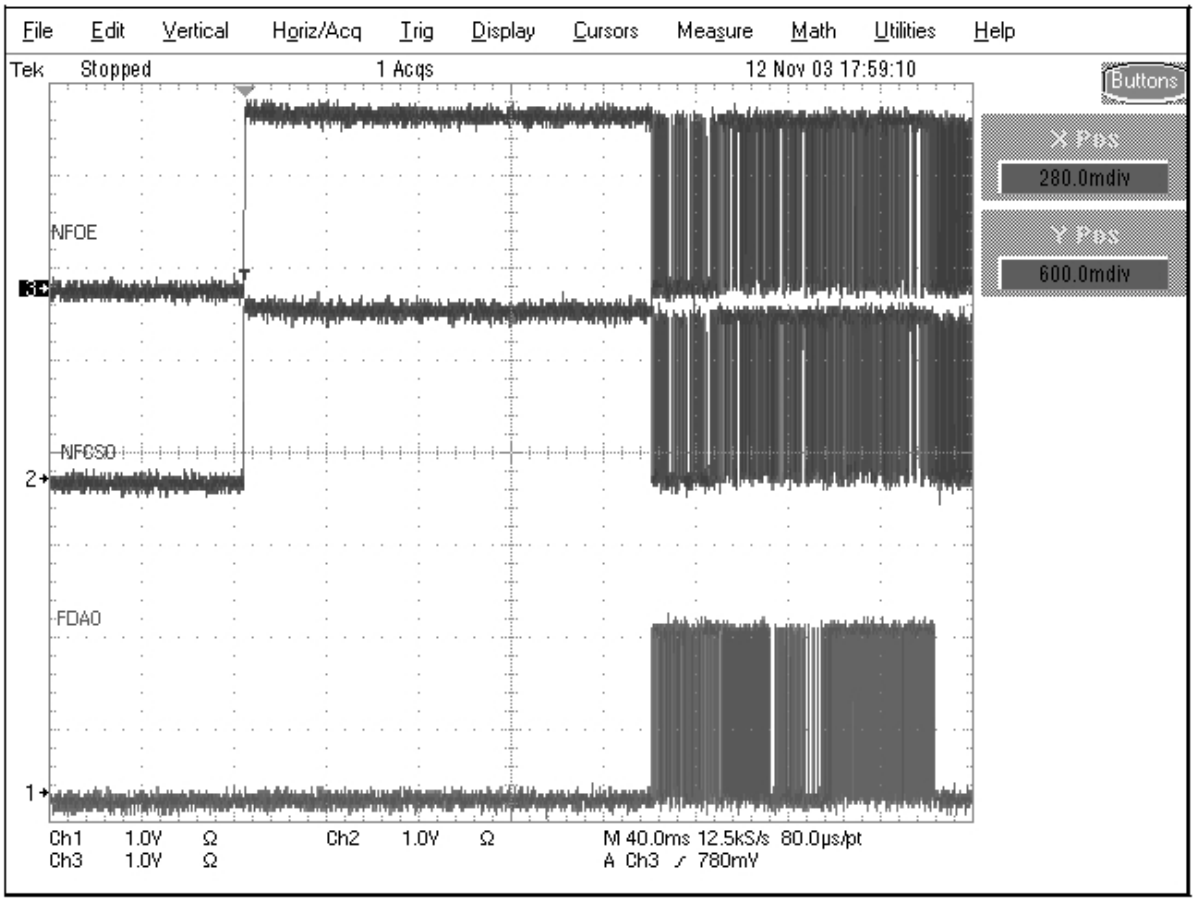

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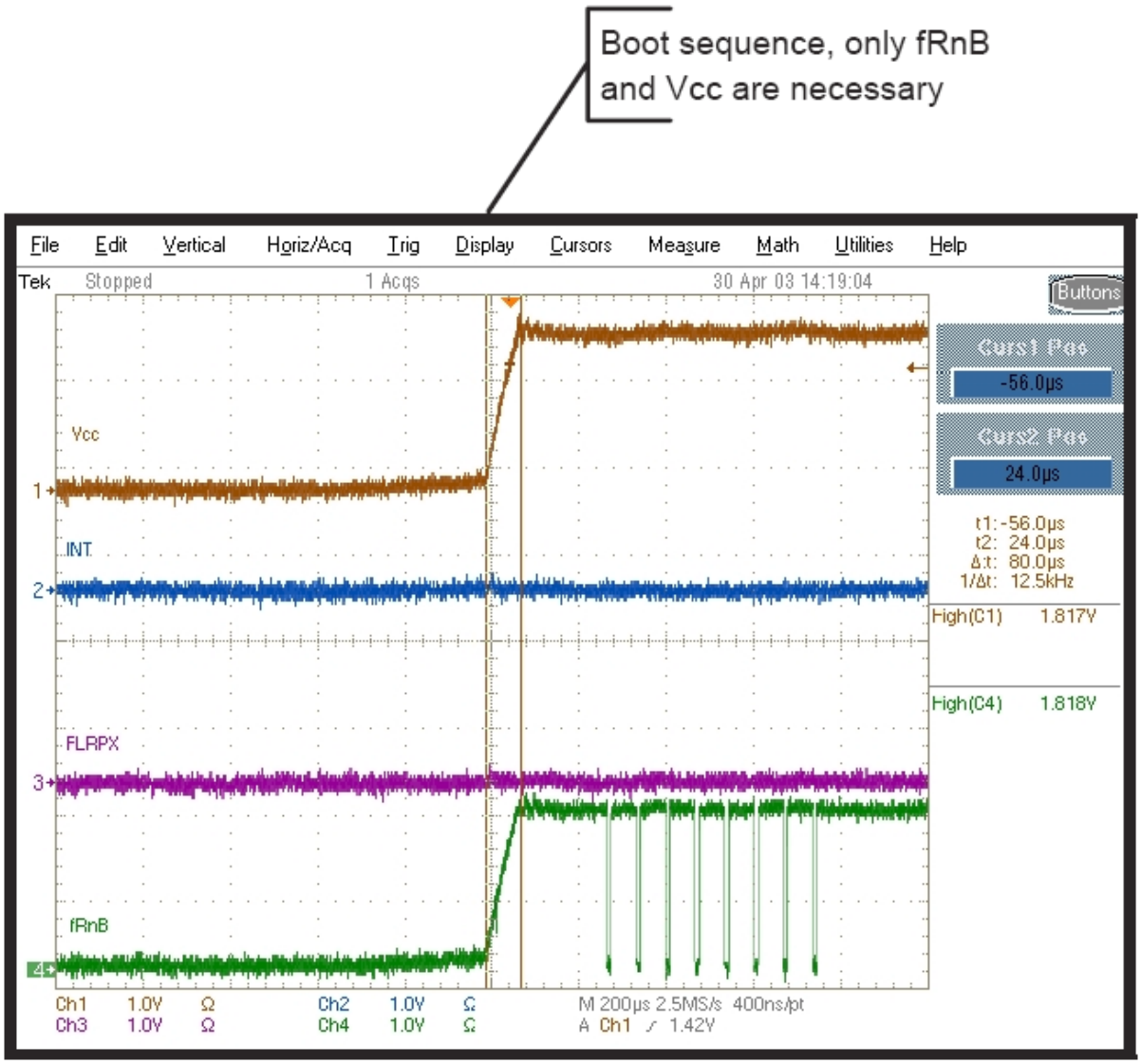
Figure 20:Oscilloscope signals



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OMAP1510 SDRAM

Figure 21:OMAP1510 SDRAM (1/2)

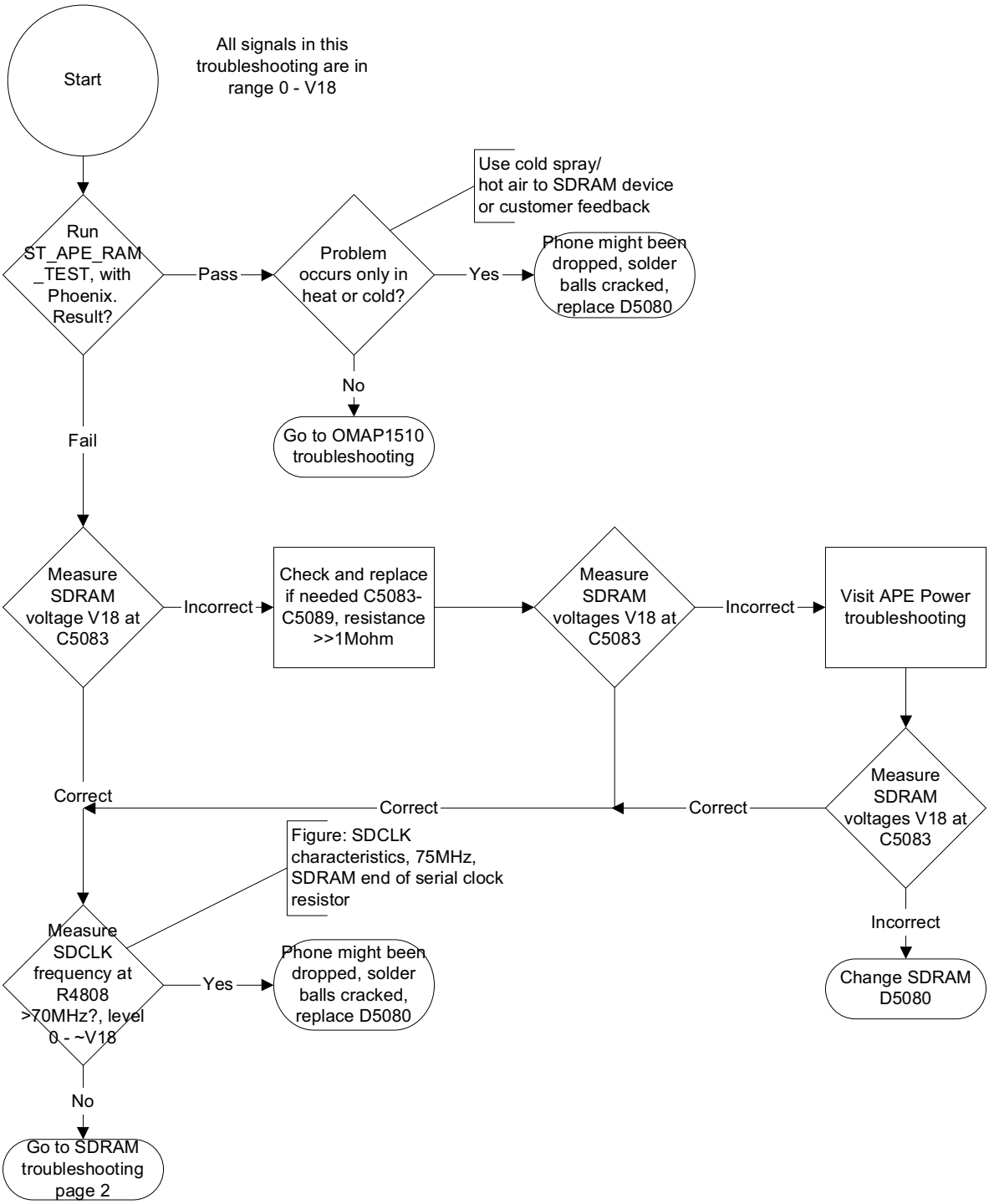
Start
All signals in this troubleshooting are in range 0 - V18
Run ST_APE_RAM _TEST, with Phoenix. Result?
Pass
Problem occurs only in heat or cold?
Use cold spray/ hot air to SDRAM device or customer feedback
Yes
Phone might been dropped, solder balls cracked, replace D5080
No
Go to OMAP1510 troubleshooting
Fail
Measure SDRAM voltage V18 at C5083
Incorrect
Check and replace if needed C5083-C5089, resistance >>1Mohm
Measure SDRAM voltages V18 at C5083
Incorrect
Visit APE Power troubleshooting
Measure SDRAM voltages V18 at C5083
Correct
Correct
Correct
Incorrect
Change SDRAM D5080
Figure: SDCLK characteristics, 75MHz, SDRAM end of serial clock resistor
Measure SDCLK frequency at R4808 >70MHz?, level 0 - ~V18
Yes
Phone might been dropped, solder balls cracked, replace D5080
No
Go to SDRAM troubleshooting page 2

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Figure 22:OMAP1510 SDRAM (2/2)

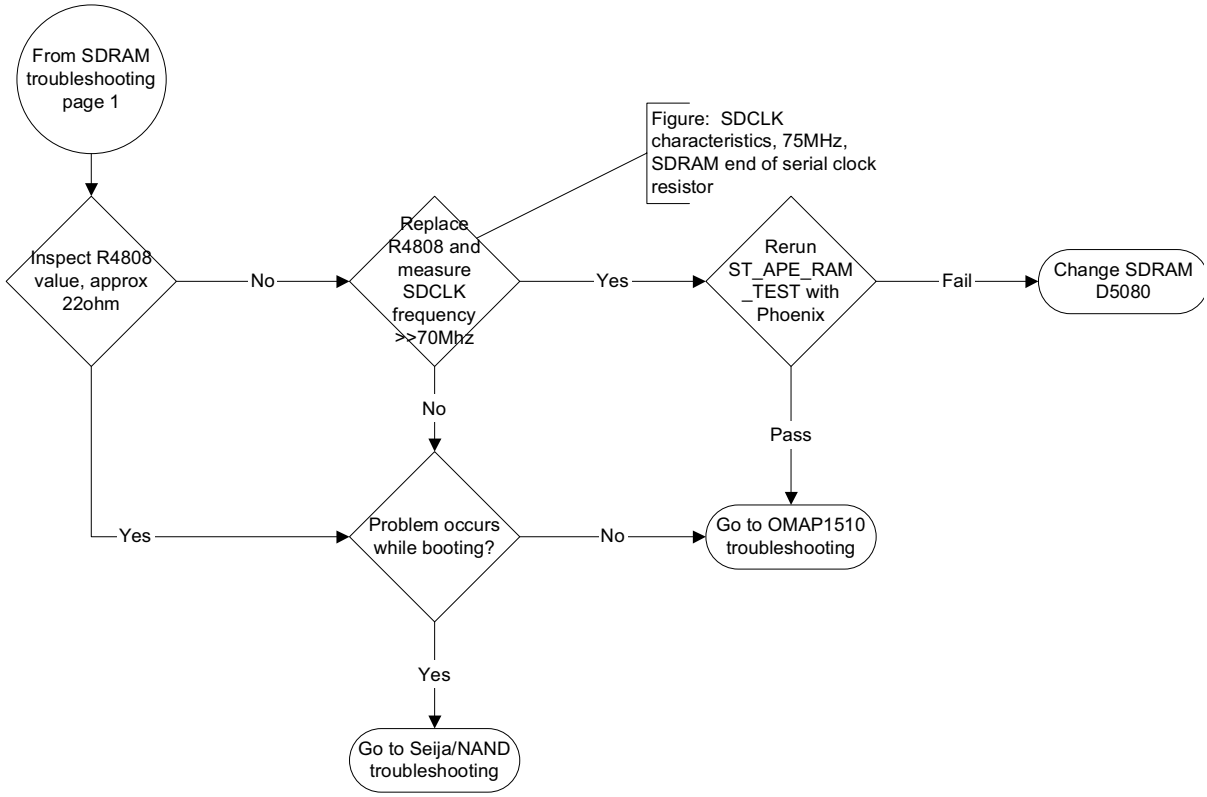

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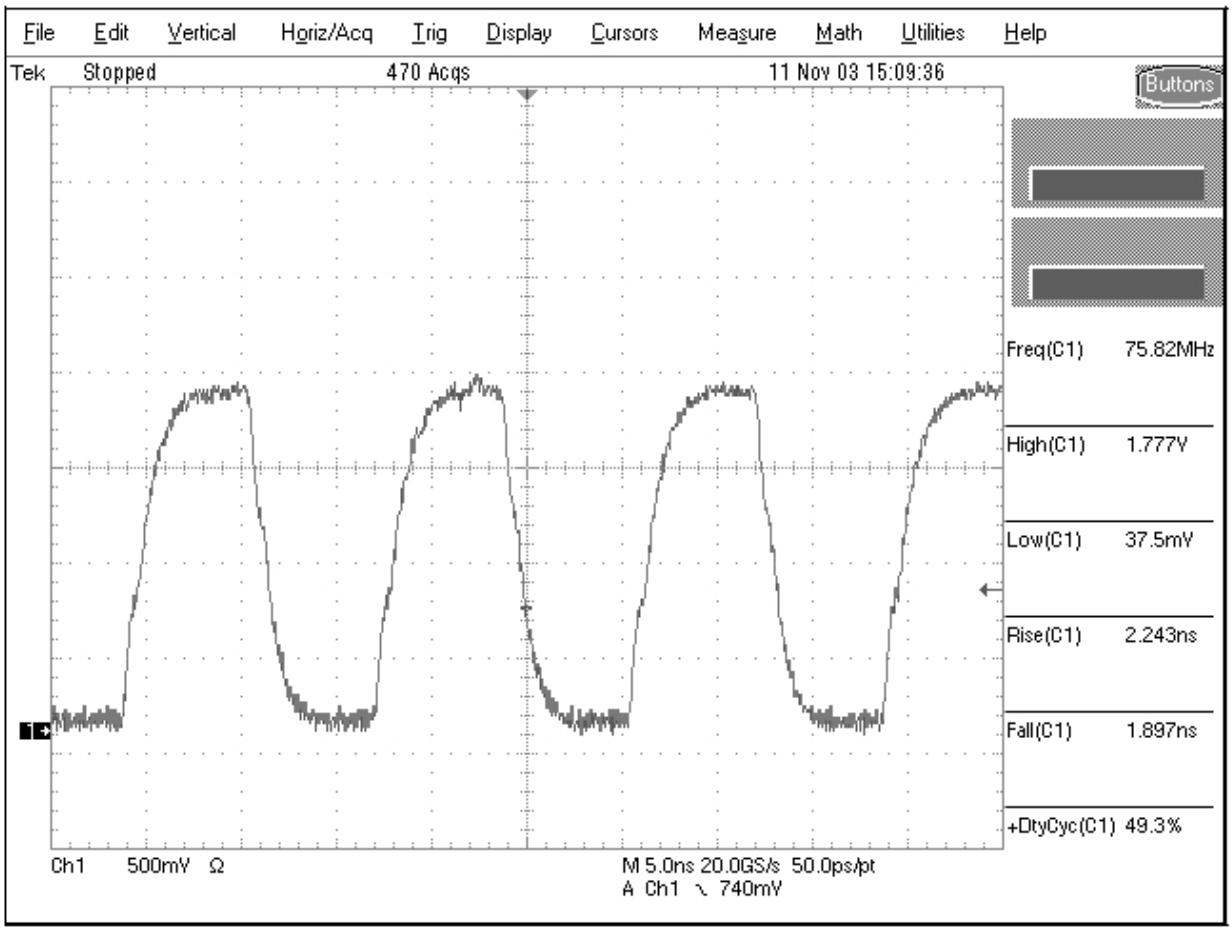
Figure 23:SDCLK characteristics, 75MHz, SDRAM end of serial clock resistor



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Energy management troubleshooting

Device does not stay on

If the device turns off without any visible reason, there may be problems in the following areas:

- UEM watchdog (WD) problem (WD is not updated by SW)
- BSI line problem (BSI line is floating => contact failure)
- Battery line problem
- Soldering problem

The most likely reason is UEM WD, which turns the device off after about 32 seconds if SW is jammed.

This may caused by a software problem, UPP8M problem (Not served by SW), UEM or memory malfunctions.

The following tests are recommended:

- General power checking
- Clocks
- Memory testing
- Serial Interface

If there is something wrong in the BSI line, the device seems to be dead after the power key is pressed. However the regulators of the device are on a few seconds before the power down mode.

This mode can easily be detected from the current consumption of the device. After a few seconds the current consumption drops almost to 0 mA.

In this case check the following components and/or their soldering:

- Battery connector X2020
- BSI pull up R2201 and series resistor R2202
- UEM D2200 (pin number C2)

If the phone boots to TEST or LOCAL mode with a normal battery, BSI is short circuited to ground. Check EMI-filter and filtering capacitors, which are located in the BSI.

General power checking

For power checking, use service tool SF-8.

Battery voltage should be at least 3.6V.

After disassembling the phone, use module jig MJ-13.

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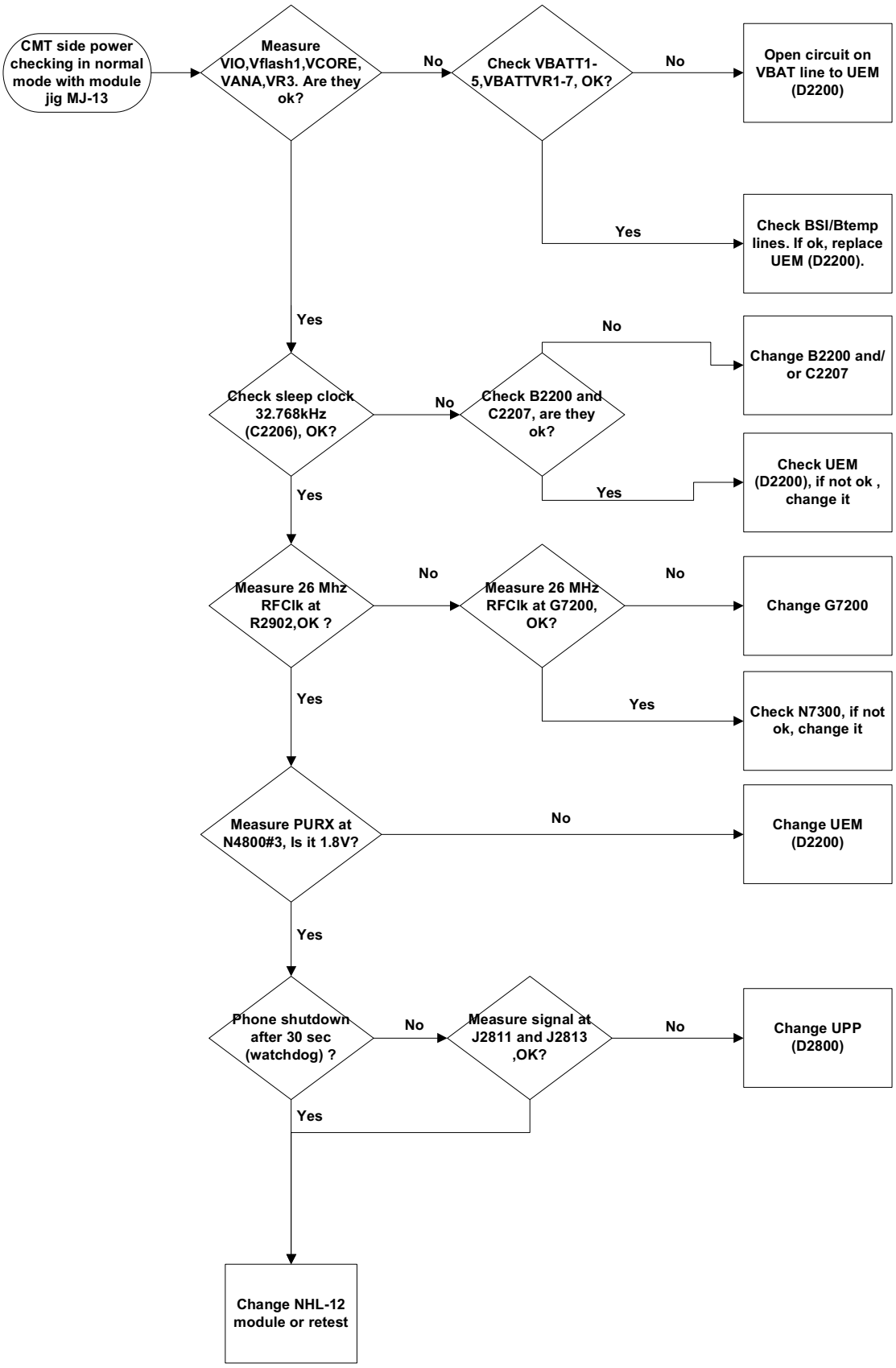
Figure 24:General power checking.



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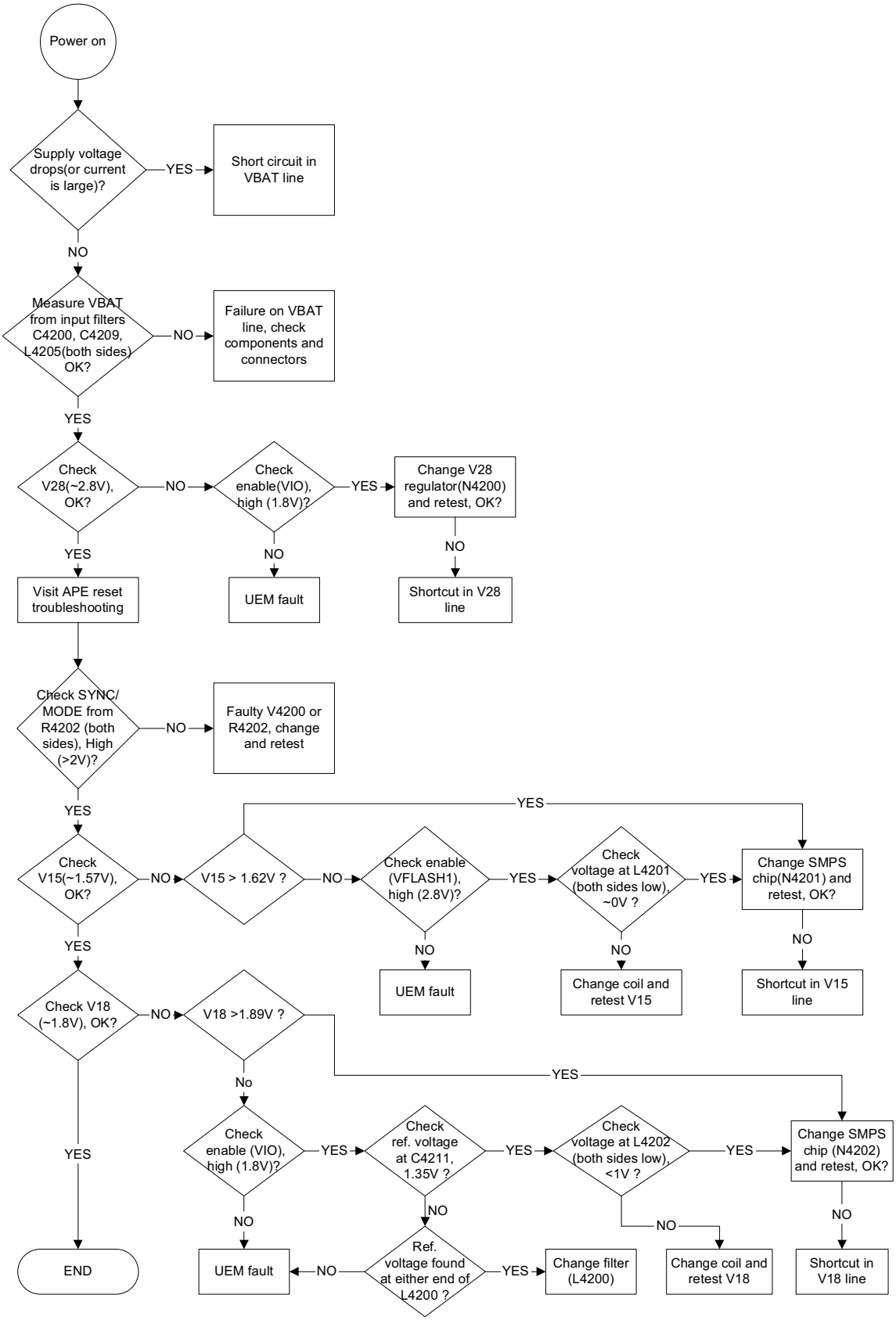
APE power checking (SMPS)



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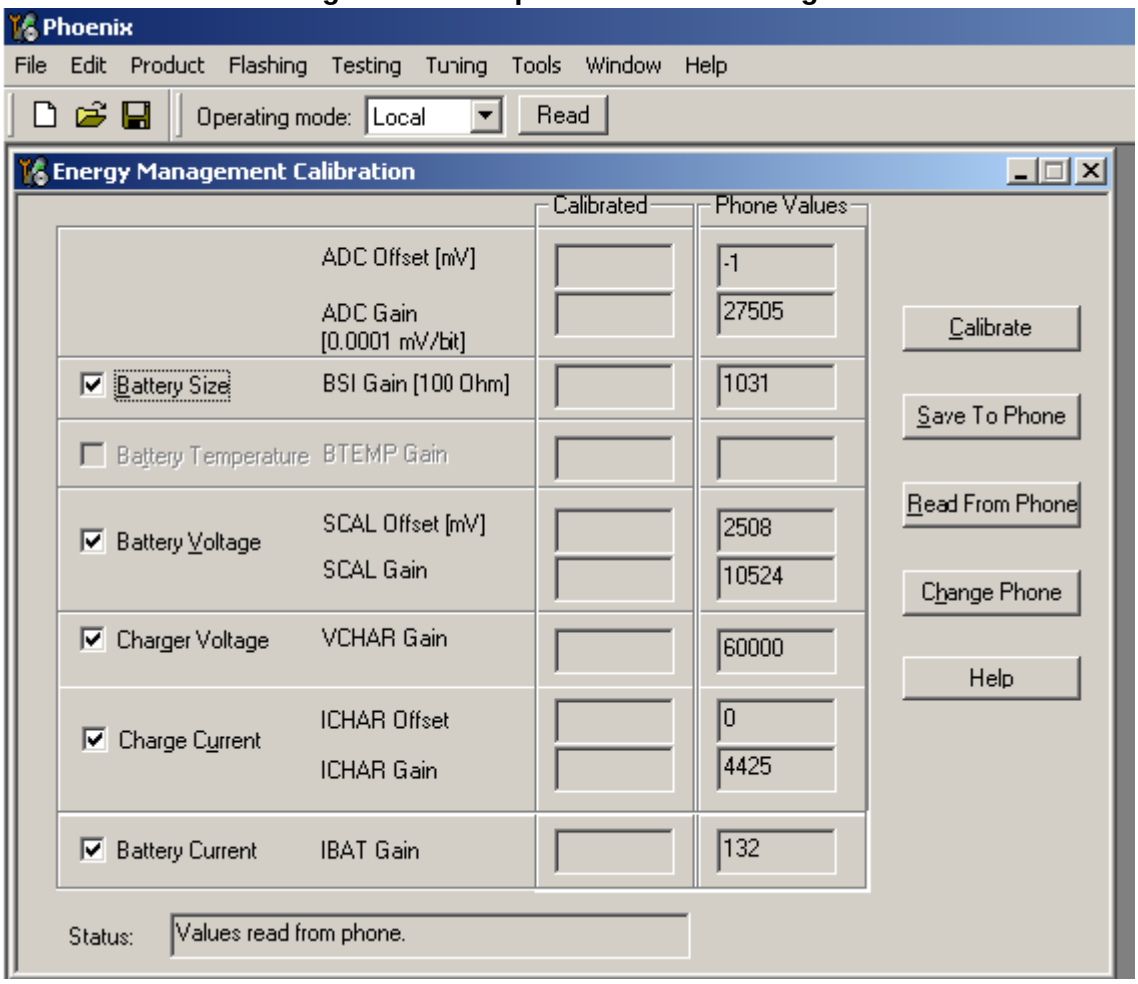
Energy management calibration

During energy management calibration, A/D-converter, BSI, BTEMP, Battery Voltage, Charger Voltage and Charger Current are calibrated

Figure 25:Example of Phoenix settings:



Limits for calculated calibration values are as follows:

Table 26: Limits for calibration values

Channel	Low	High
ADC Offset	-50	50
ADC Gain	25400	29500
BSI Gain	970	1100
Vbatt Offset	2300	2900
Vbatt Gain	10000	11000
Vchar	58000	63000
Ichar	4050	4800

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Table 26: Limits for calibration values

Channel	Low	High
Ibat	80	150

If ADC Offset is over limits: Inspect the BSI line and its components (R2202, Pull-up resistor R2201). If these are OK, change the UEM.

If BSI Gain is over limits: Inspect the BSI line and its components (R2202, Pull-up resistor R2201). If these are OK, change the UEM.

If Vbatt Offset and Gain are over limits: Inspect Vbatt lines and its components.

If Vchar is over limits: Inspect components, which are connected to the Vchar line: V2020, F2020 and L2020

If Ichar is over limits: Inspect components which are connected at Vchar line. If those are OK, First change current sense resistor (R2200), if calibration is not successful, change the UEM.

You can check calibration by using ADC-readings. Known voltages, currents and resistance are fed and read by ADC-readings. These read values and known values can be compared.

ADC-reading

Divided and scaled battery voltage, Charger voltage, Charger current, BSI and Btemp values can be read by this tool. Read values a few times before you can be sure that results are accurate.

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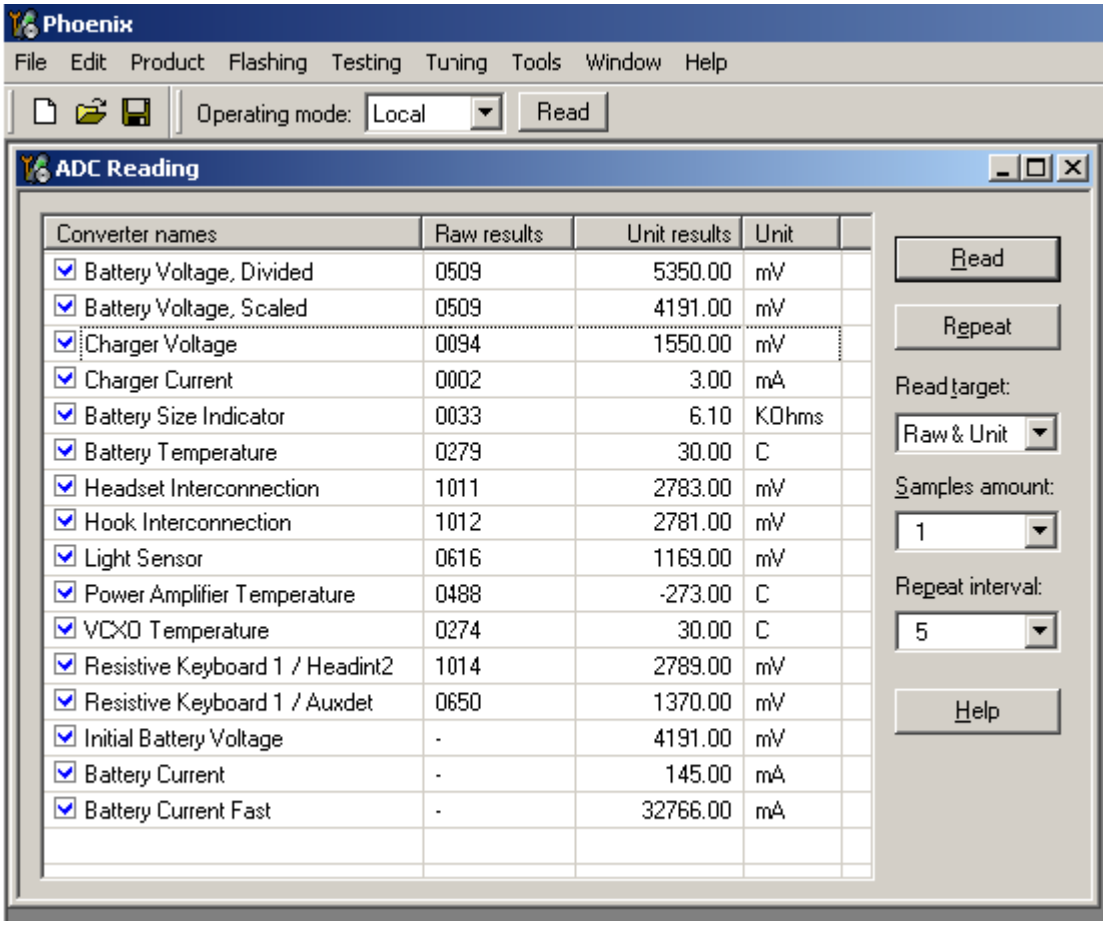
Figure 26:ADC Reading window


Phoenix
File Edit Product Flashing Testing Tuning Tools Window Help
Operating mode: Local
Read
ADC Reading
Converter names | Raw results | Unit results | Unit
Battery Voltage, Divided | 0509 | 5350.00 | mV
Battery Voltage, Scaled | 0509 | 4191.00 | mV
Charger Voltage | 0094 | 1550.00 | mV
Charger Current | 0002 | 3.00 | mA
Battery Size Indicator | 0033 | 6.10 | KOhms
Battery Temperature | 0279 | 30.00 | C
Headset Interconnection | 1011 | 2783.00 | mV
Hook Interconnection | 1012 | 2781.00 | mV
Light Sensor | 0616 | 1169.00 | mV
Power Amplifier Temperature | 0488 | -273.00 | C
VCXO Temperature | 0274 | 30.00 | C
Resistive Keyboard 1 / Headint2 | 1014 | 2789.00 | mV
Resistive Keyboard 1 / Auxdet | 0650 | 1370.00 | mV
Initial Battery Voltage | - | 4191.00 | mV
Battery Current | - | 145.00 | mA
Battery Current Fast | - | 32766.00 | mA
Read
Repeat
Read target:
Raw & Unit
Samples amount:
1
Repeat interval:
5
Help

NOTE: IF Vbatt Scaled and Divided unit results are different default calibration values are used. In this case perform EM-calibration to get full performance of the phone.

Table 27: Maximum reading tolerances

Reading	Check point	Tolerance
Vbatt SCAL_	4.2V	± 25mV
Vchar	8.4V	± 40mV
Ichar	500mA	± 20mA
BSI	75k	± 1.3kohm
Btemp	273K(47k)	± 5K

Backup battery

If there is a backup battery fault, one of the symptoms is Real Time Clock losing the correct time during short main battery removal.

The same symptom may also occur when the backup battery is empty. About 5 hours is needed to fully charge the backup battery.

NOTE: Backup battery is only charged at the same time as the main battery or when the device is in either LOCAL or TEST mode.

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Always check the backup battery visually for any leakage or any other visual defect.

Check that the backup battery is correctly mounted in the device before closing the cover.

Check with Phoenix that backup battery is OK.

Measure the voltage of backup battery:

- Normal operation when the voltage is > 2.0V
- Fully charged when the voltage is about 3.2V (because of large internal impedance voltage won't stay above 3.0V a long time after charging is disabled)

Enable backup battery charging (start to charge main battery or boot device to LOCAL or TEST mode).

Measure the voltage of the backup battery during charging. It should rise, if it is not 3.2V, yet.

When the voltage is over 2.0V for sure, check the backup battery with Phoenix. If not OK, then D2200 is probably faulty.

Ensure that the RTC is running.

Charging troubleshooting

Use the BL5-C battery and JBV-1 calibration set to test charging.

NOTE: power supply cannot be charged, if it does not have a current sinking capability.

When you are charging a totally empty battery, remember that start-up charging might take a little bit longer time than normally. During this time the display is blank.

If a charger is not of Nokia approved type and its current and voltage are not within Nokia charger window, software does not start charging and "NOT CHARGING" is displayed. The voltage should be between 5.3V - 9.5V and current between 200mA – 900mA

Remove and reconnect the battery and charger a few times before you start to measure the device. This check ensures that the fault really exists.

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Figure 27:Charging troubleshooting (1/2)

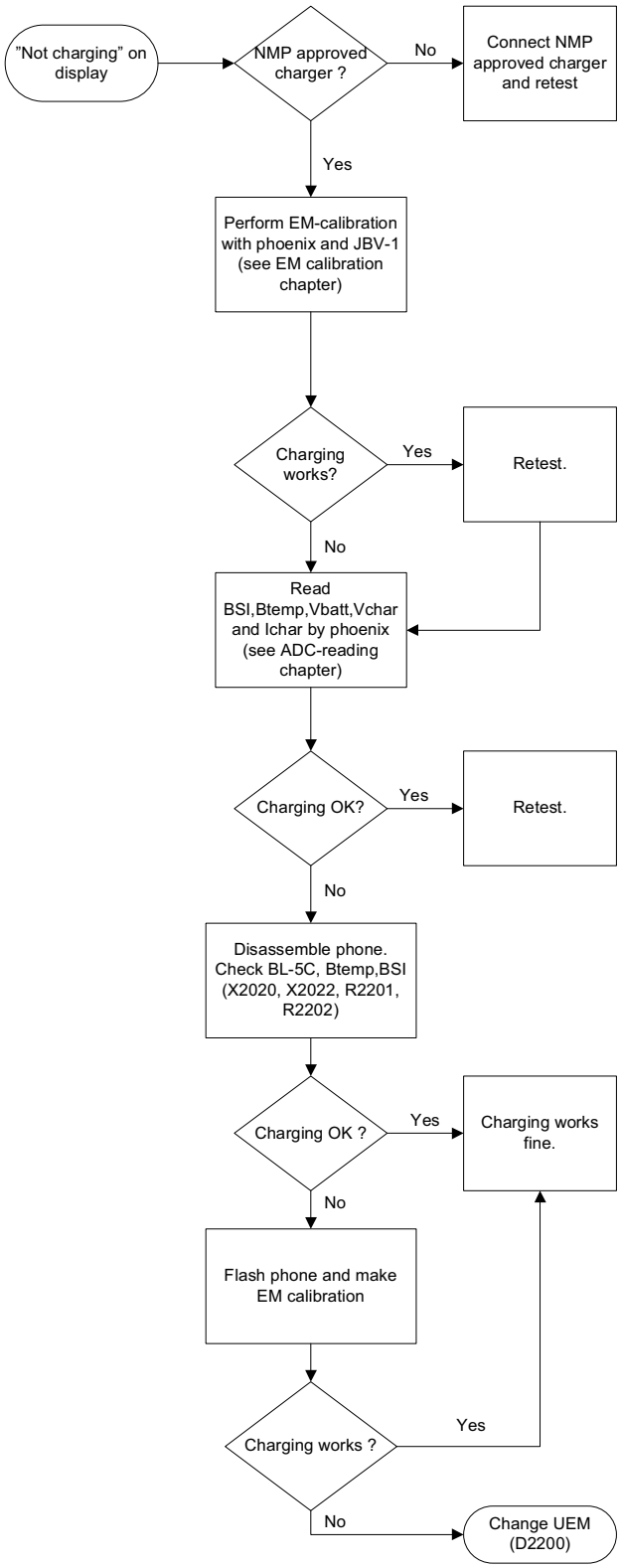

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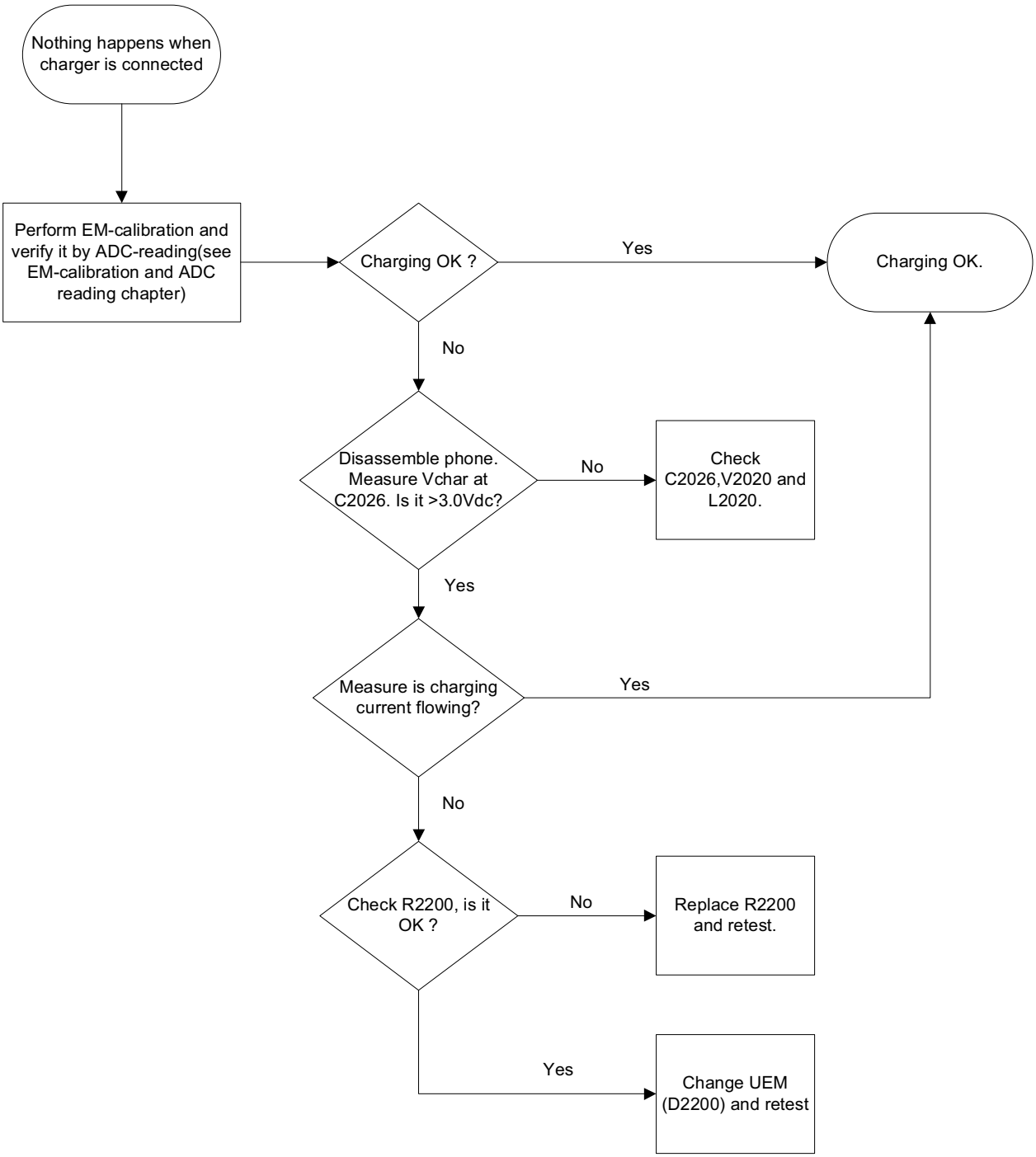
Figure 28:Charging troubleshooting (2/2)



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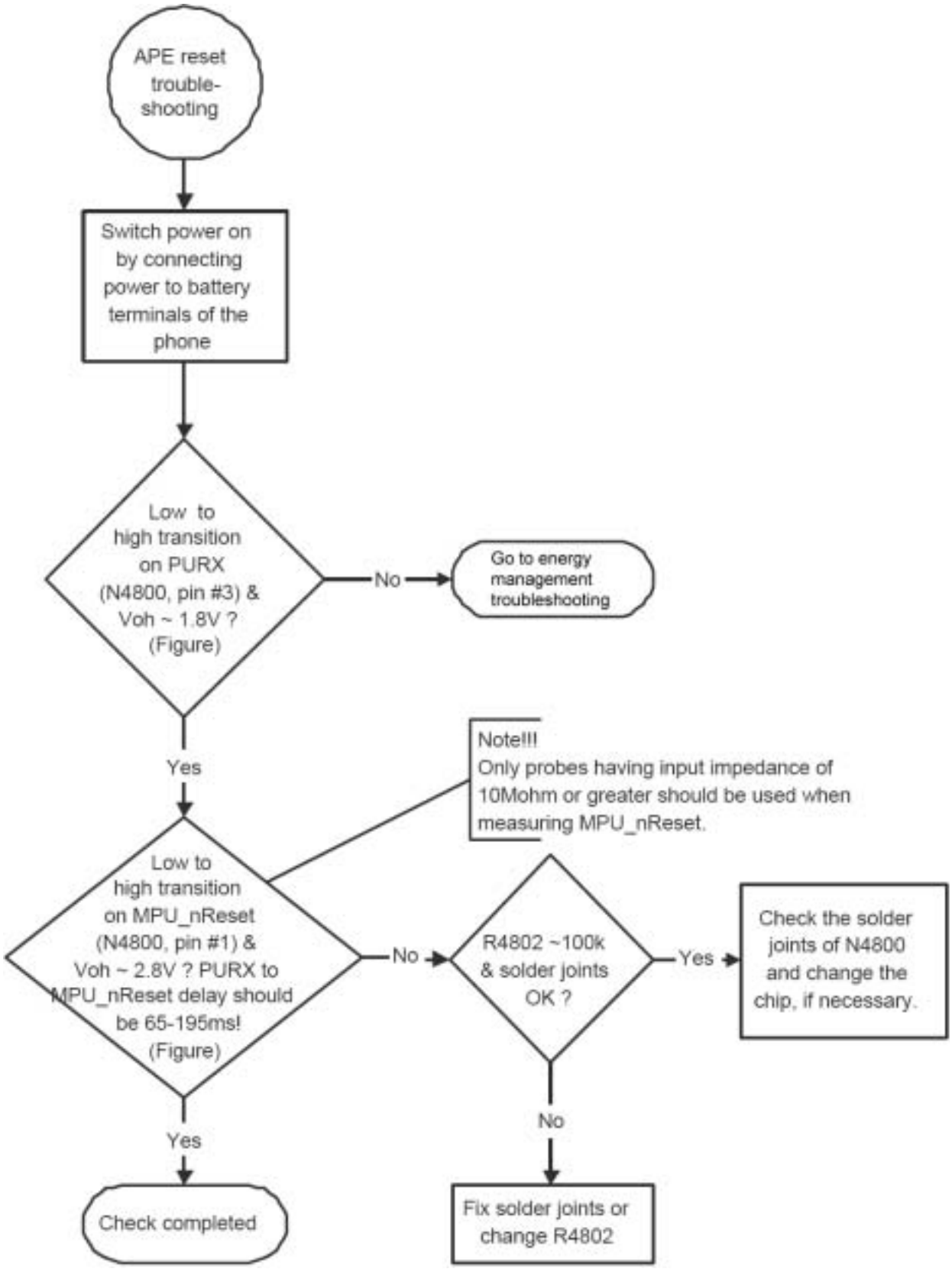
APE reset


APE reset trouble-shooting
Switch power on by connecting power to battery terminals of the phone
Low to high transition on PURX (N4800, pin #3) & Voh ~ 1.8V ? (Figure)
No
Go to energy management troubleshooting
Yes
Note!!!
Only probes having input impedance of 10Mohm or greater should be used when measuring MPU_nReset.
Low to high transition on MPU_nReset (N4800, pin #1) & Voh ~ 2.8V ? PURX to MPU_nReset delay should be 65-195ms! (Figure)
No
R4802 ~100k & solder joints OK ?
Yes
Check the solder joints of N4800 and change the chip, if necessary.
No
Yes
Check completed
Fix solder joints or change R4802

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OMAP1510 (Helen)

Figure 29:OMAP1510 (Helen) (1/2)

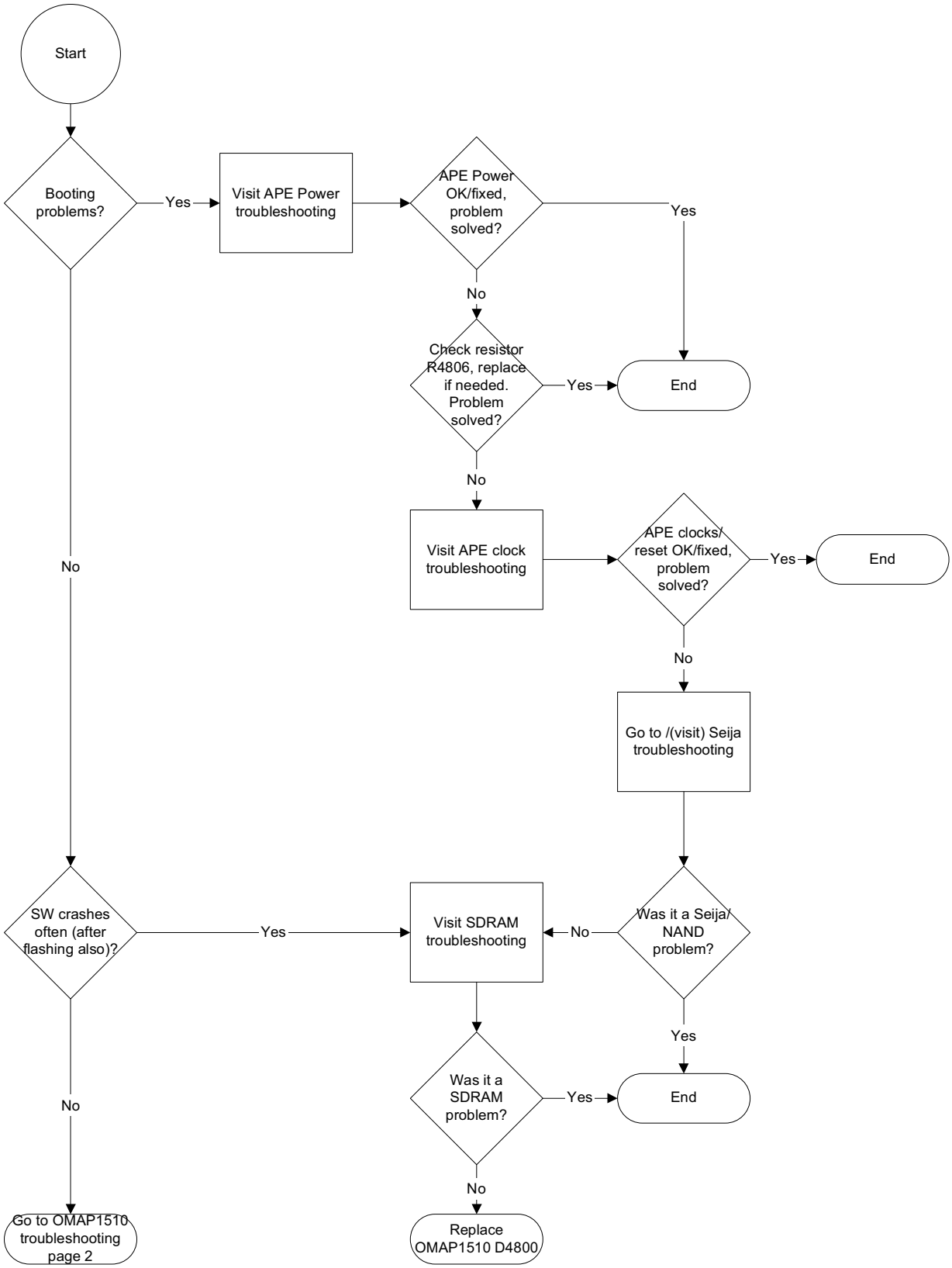

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Figure 30:OMAP1510 (Helen) (2/2)

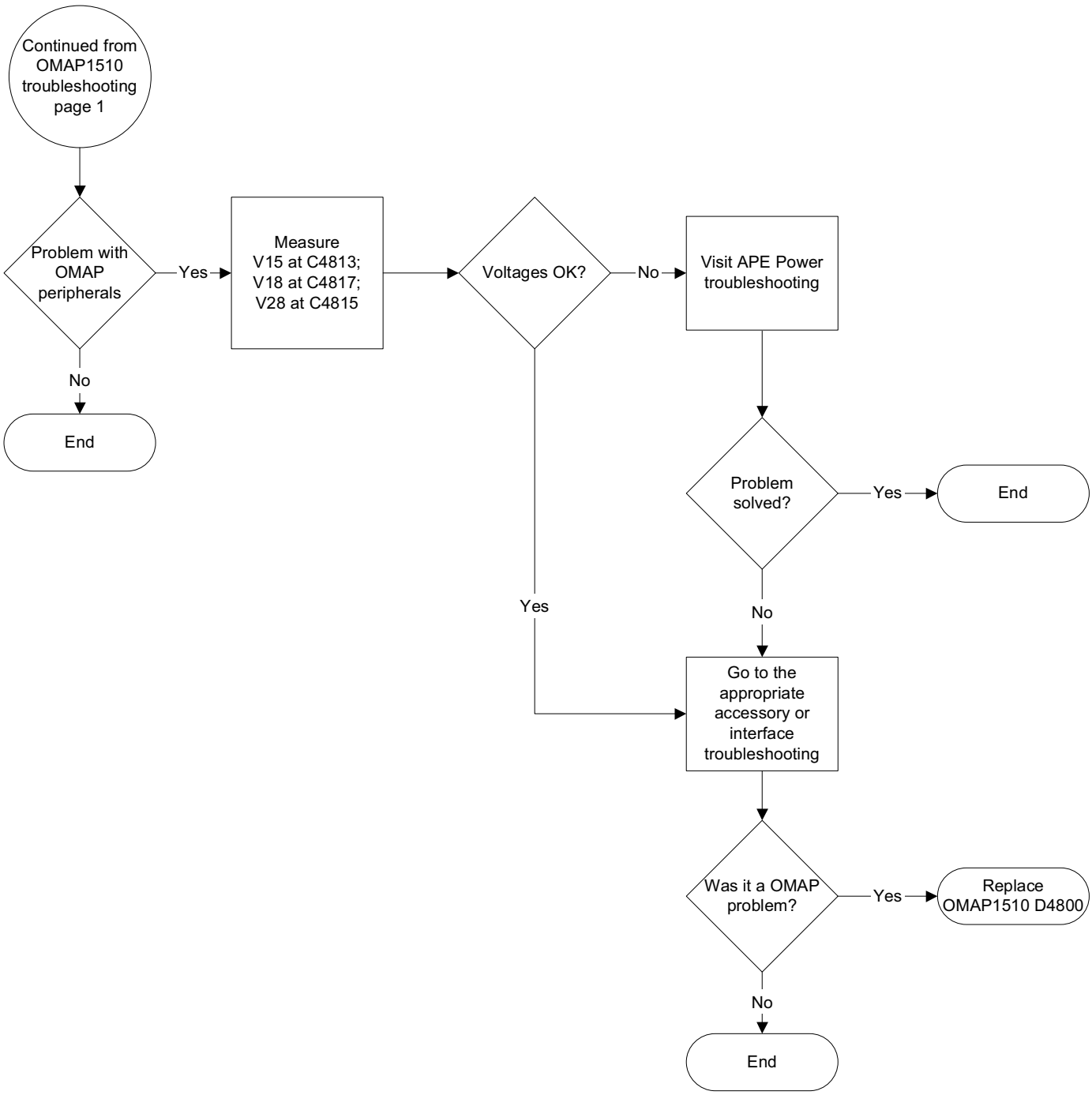

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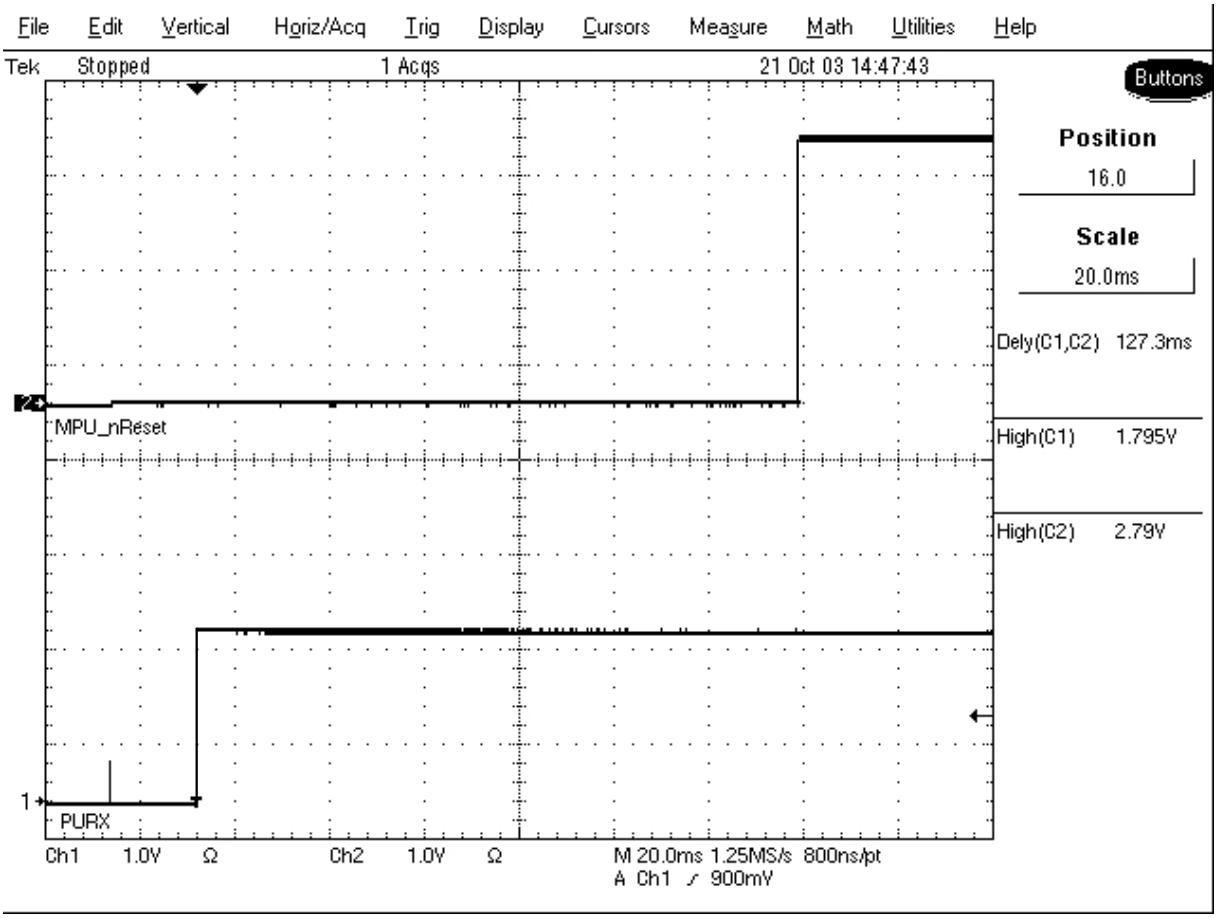
Figure 31:Reset signals (PURX and MPU_nReset)



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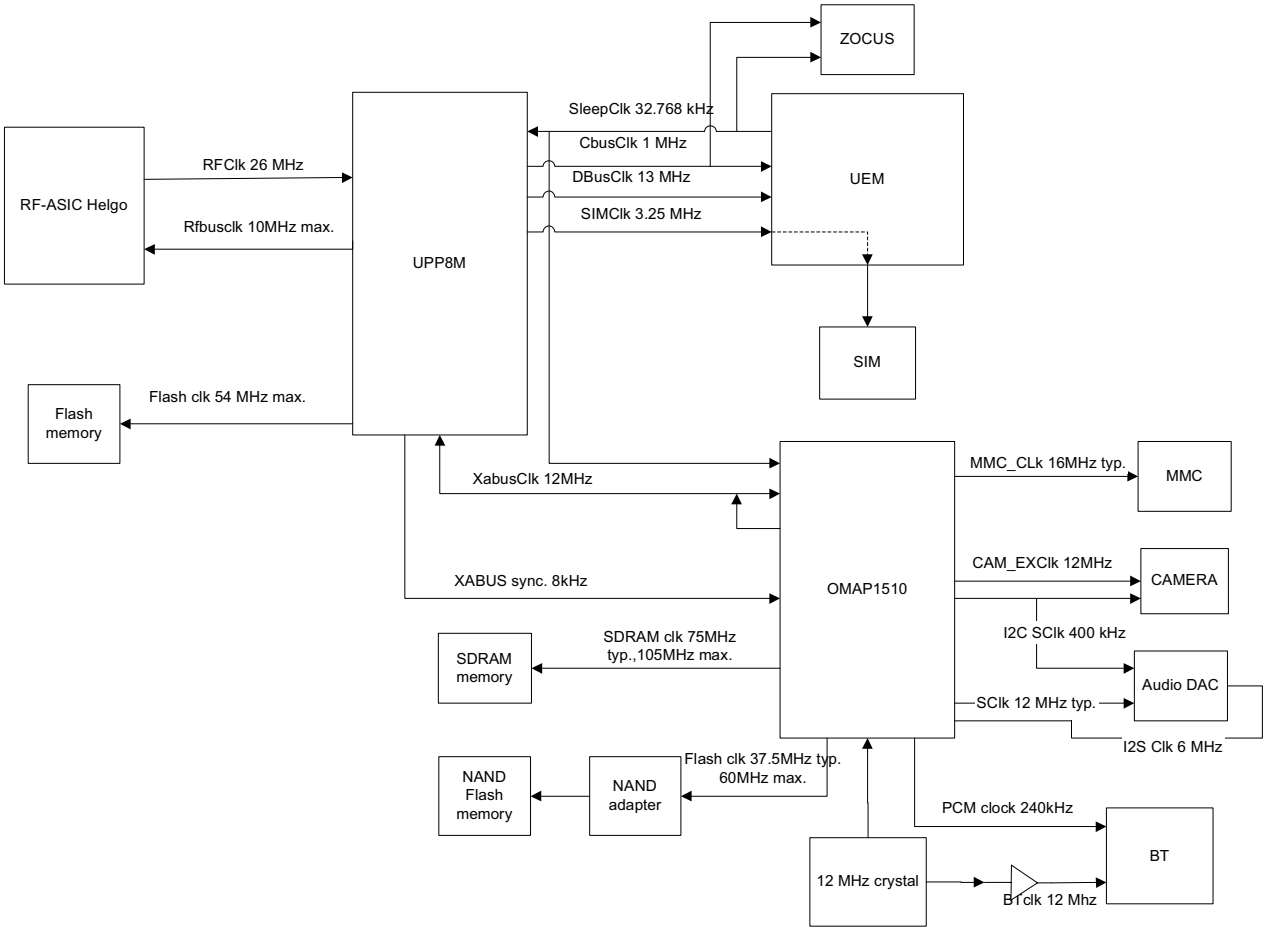
Clocks troubleshooting

Clocks include the following:

- RF clock
- CAMclkDBUS
- CBUS clocks
- Flash and SDRAM clocks
- Sleep clock
- Bluetooth clock
- SIM clock
- MMC clock
- XABUS
- Camera
- Audio

Figure 32:NHL-12 clocks



The main clock signal for the CMT is generated from the voltage controlled crystal oscillator VCTCXO. This 26 MHz triangle wave clock signal is supplied to OSC_IN pin of Helgo and out to UPP8M. Inside the UPP8M, the clock frequency is divided to 13 MHz and then fed to RFCLK.

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In SLEEP mode, the VCTCXO is off. UEM generates a low frequency clock signal (32.768 kHz) that is fed to UPP8M and ZOCUS.

When the flashing of the device does not succeed, but powering is OK, follow these instructions.

Note: The absence of clocks may indicate that the device (set phone to LOCAL mode when the sleep is not allowed or press buttons so that phone is not in sleep mode) is in sleep mode. Make sure that the device is not in sleep during clocks measuring.

IMPORTANT: Clock signals have to be measured with 1MW (or greater) probes!

- Measure signal from G7200. This should be 26Mhz clock signal.
- Check that the crystal oscillator (B2200) is oscillating at 32.768kHz frequency. If not, change B2200. If OK, measure sleepclk from test point J2802. Frequency should be the same, 32.678kHz. If not, change the UEM.

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Figure 33:APE clocks troubleshooting flowchart

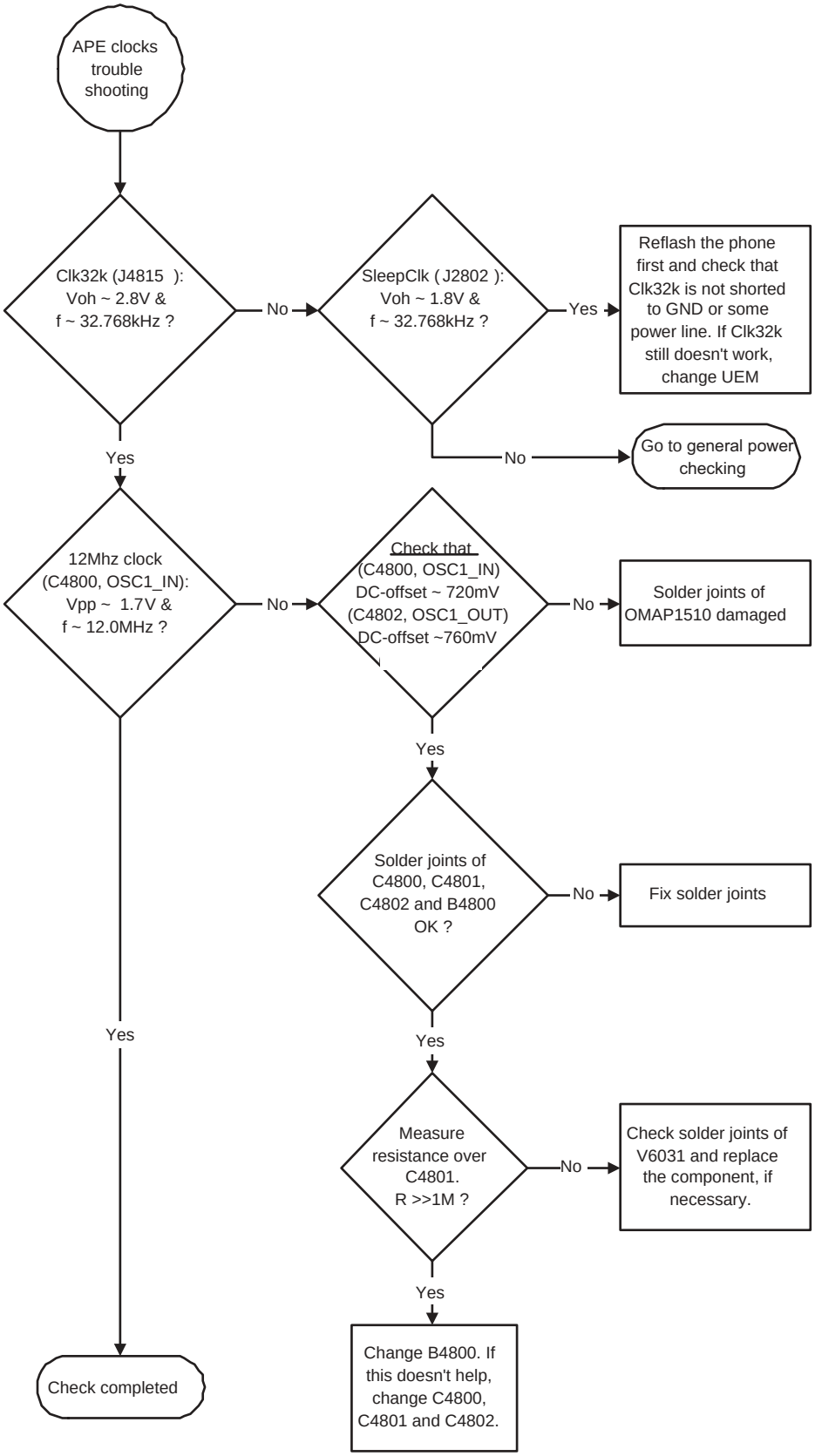
APE clocks trouble shooting
Clk32k (J4815): Voh ~ 2.8V & f ~ 32.768kHz ?
No
SleepClk (J2802): Voh ~ 1.8V & f ~ 32.768kHz ?
Yes
Reflash the phone first and check that Clk32k is not shorted to GND or some power line. If Clk32k still doesn't work, change UEM
No
Go to general power checking
Yes
12Mhz clock (C4800, OSC1_IN): Vpp ~ 1.7V & f ~ 12.0MHz ?
No
Check that (C4800, OSC1_IN) DC-offset ~ 720mV (C4802, OSC1_OUT) DC-offset ~760mV
No
Solder joints of OMAP1510 damaged
Yes
Solder joints of C4800, C4801, C4802 and B4800 OK ?
No
Fix solder joints
Yes
Measure resistance over C4801. R >>1M ?
No
Check solder joints of V6031 and replace the component, if necessary.
Yes
Change B4800. If this doesn't help, change C4800, C4801 and C4802.
Yes
Check completed

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Figure 34: Sleep clock

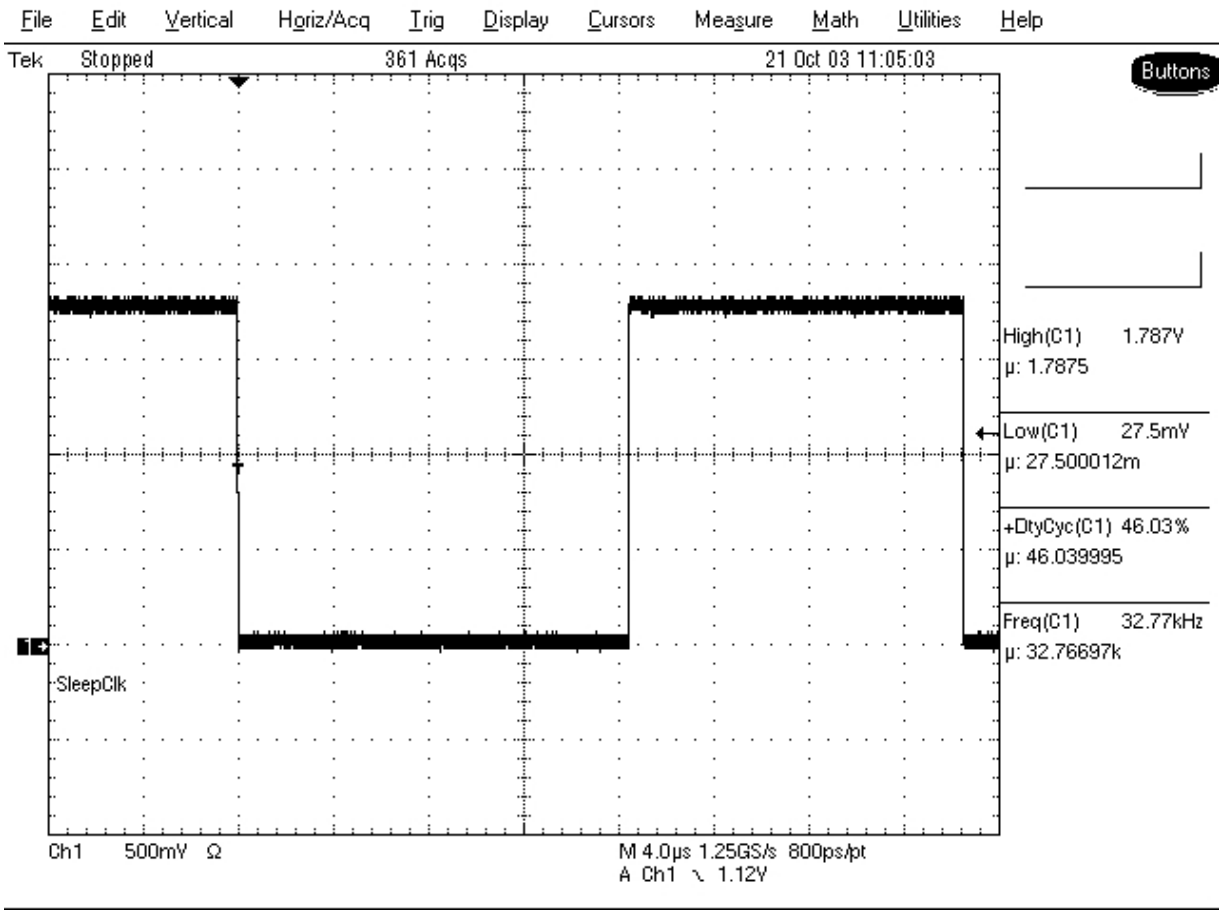

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Figure 35:12 MHz APE system clock (measured from the OSC1_IN pin of OMAP1510)

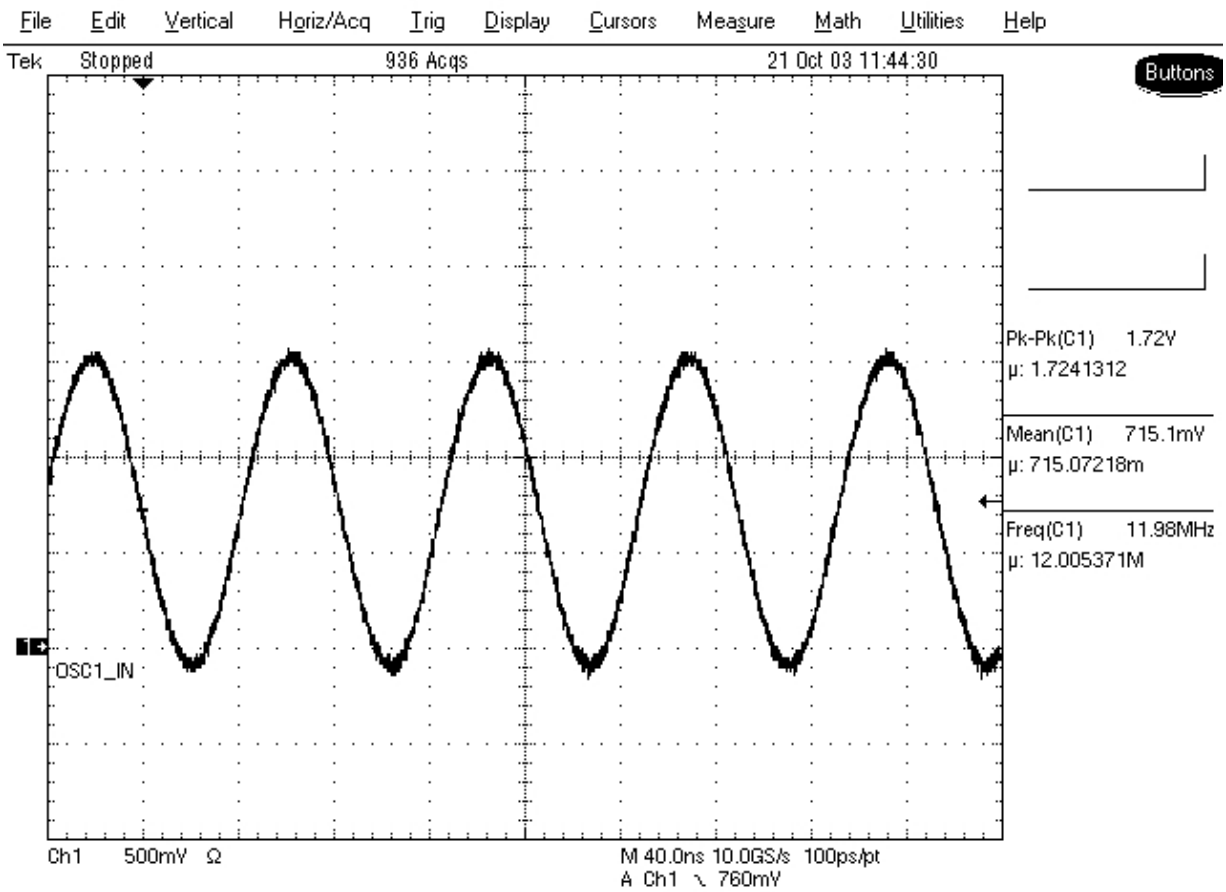

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Figure 36:12MHz APE system clock (measured from the OSC1_OUT pin of OMAP1510)

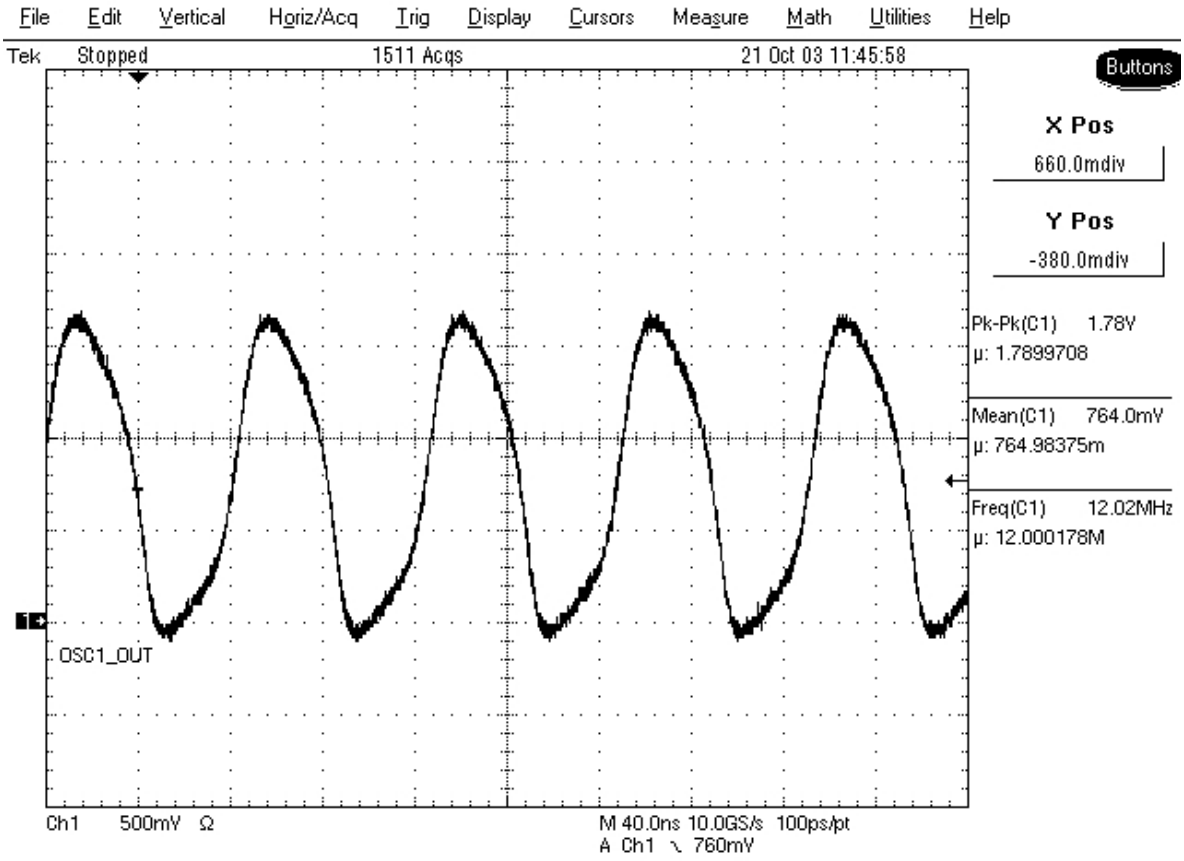

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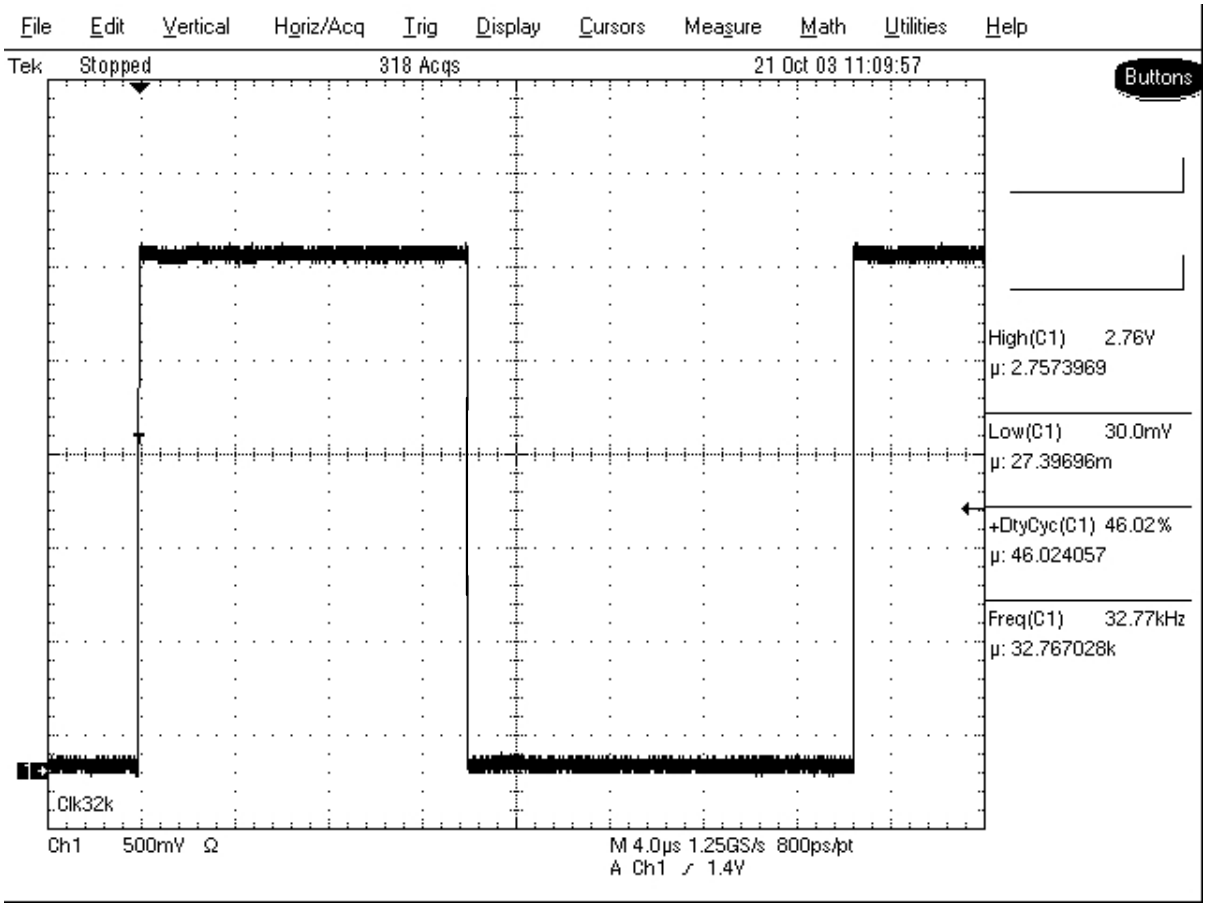
Figure 37:Clk32k



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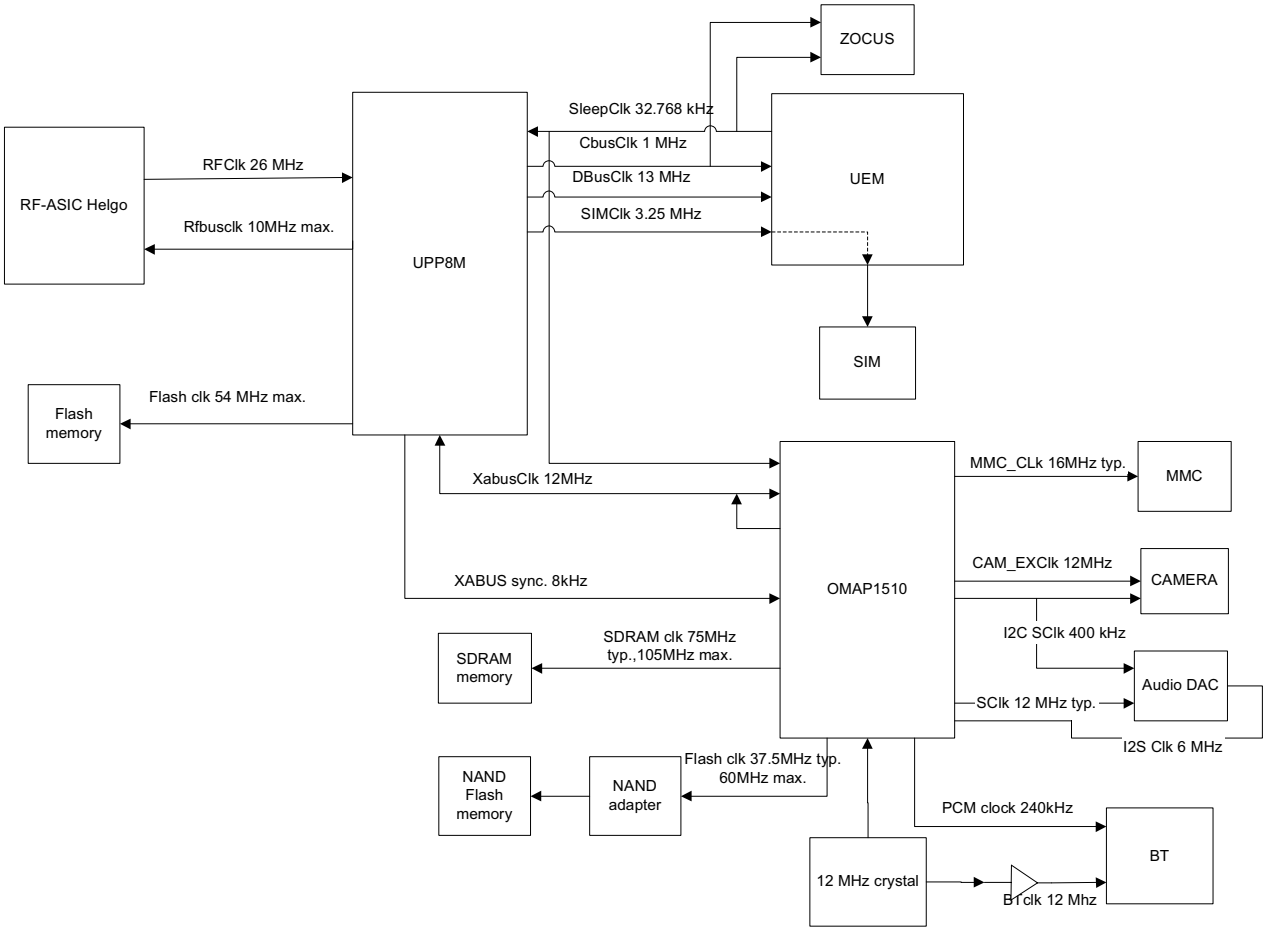
Clocks troubleshooting

Clocks include the following:

- RF clock
- CAMclkDBUS
- CBUS clocks
- Flash and SDRAM clocks
- Sleep clock
- Bluetooth clock
- SIM clock
- MMC clock
- XABUS
- Camera
- Audio

Figure 38:NHL-12 clocks



The main clock signal for the CMT is generated from the voltage controlled crystal oscillator VCTCXO. This 26 MHz triangle wave clock signal is supplied to OSC_IN pin of Helgo and out to UPP8M. Inside the UPP8M, the clock frequency is divided to 13 MHz and then fed to RFCLK.

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In SLEEP mode, the VCTCXO is off. UEM generates a low frequency clock signal (32.768 kHz) that is fed to UPP8M and ZOCUS.

When the flashing of the device does not succeed, but powering is OK, follow these instructions.

Note: The absence of clocks may indicate that the device (set phone to LOCAL mode when the sleep is not allowed or press buttons so that phone is not in sleep mode) is in sleep mode. Make sure that the device is not in sleep during clocks measuring.

IMPORTANT: Clock signals have to be measured with 1MW (or greater) probes!

- Measure signal from G7200. This should be 26Mhz clock signal.
- Check that the crystal oscillator (B2200) is oscillating at 32.768kHz frequency. If not, change B2200. If OK, measure sleepclk from test point J2802. Frequency should be the same, 32.678kHz. If not, change the UEM.

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Figure 39:APE clocks troubleshooting flowchart

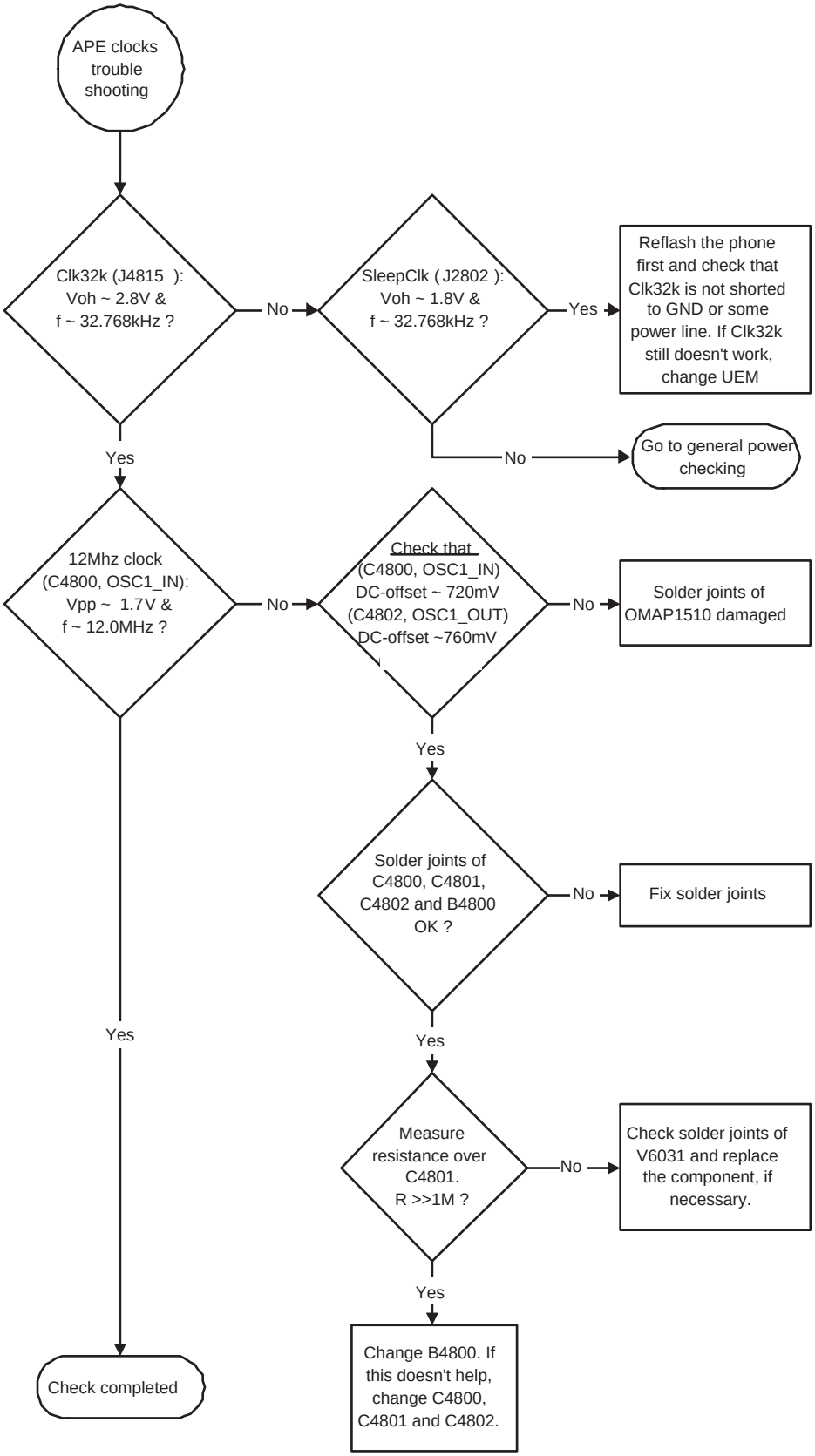
APE clocks trouble shooting
Clk32k (J4815): Voh ~ 2.8V & f ~ 32.768kHz ?
No
SleepClk (J2802): Voh ~ 1.8V & f ~ 32.768kHz ?
Yes
Reflash the phone first and check that Clk32k is not shorted to GND or some power line. If Clk32k still doesn't work, change UEM
No
Go to general power checking
Yes
12Mhz clock (C4800, OSC1_IN): Vpp ~ 1.7V & f ~ 12.0MHz ?
No
Check that (C4800, OSC1_IN) DC-offset ~ 720mV (C4802, OSC1_OUT) DC-offset ~760mV
No
Solder joints of OMAP1510 damaged
Yes
Solder joints of C4800, C4801, C4802 and B4800 OK ?
No
Fix solder joints
Yes
Measure resistance over C4801. R >>1M ?
No
Check solder joints of V6031 and replace the component, if necessary.
Yes
Change B4800. If this doesn't help, change C4800, C4801 and C4802.
Yes
Check completed

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Figure 40: Sleep clock

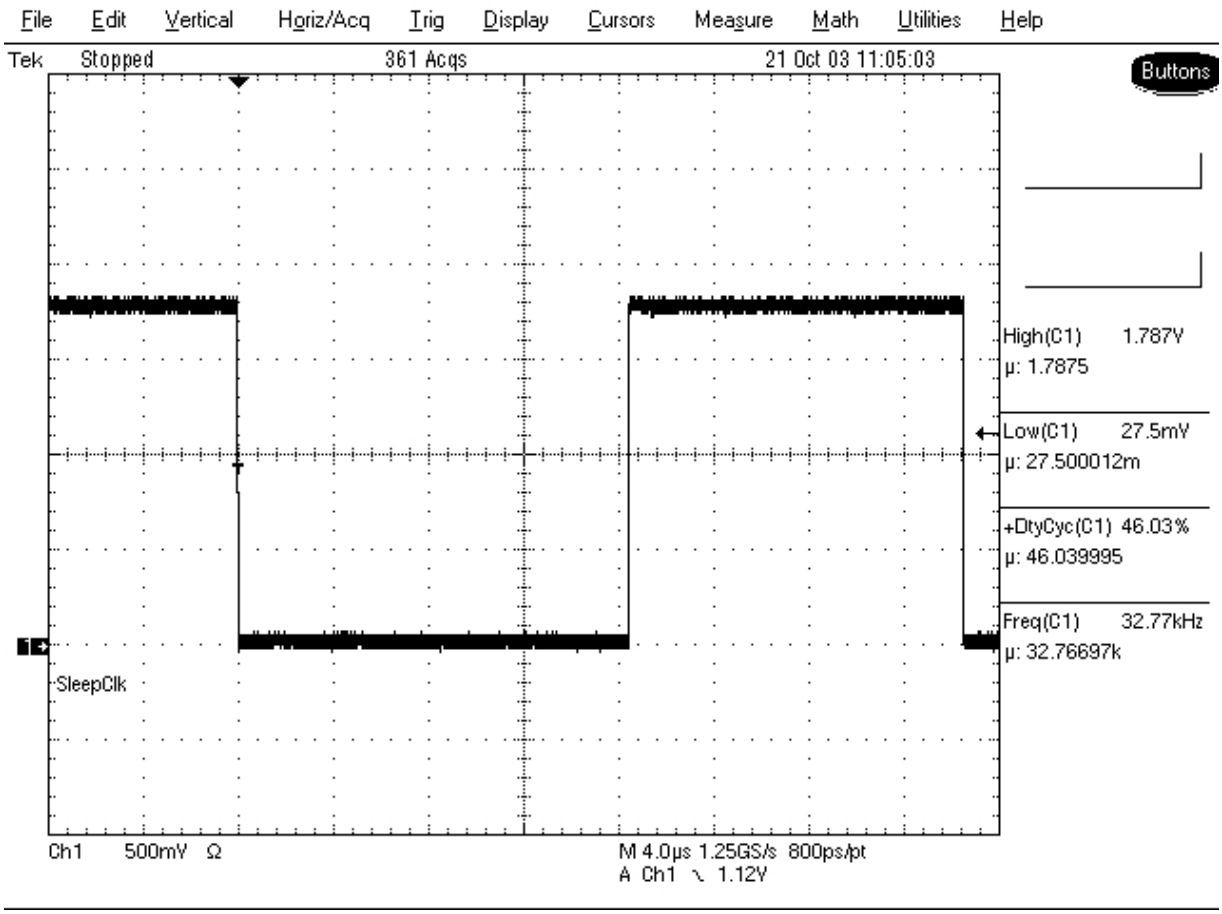

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Figure 41:12 MHz APE system clock (measured from the OSC1_IN pin of OMAP1510)

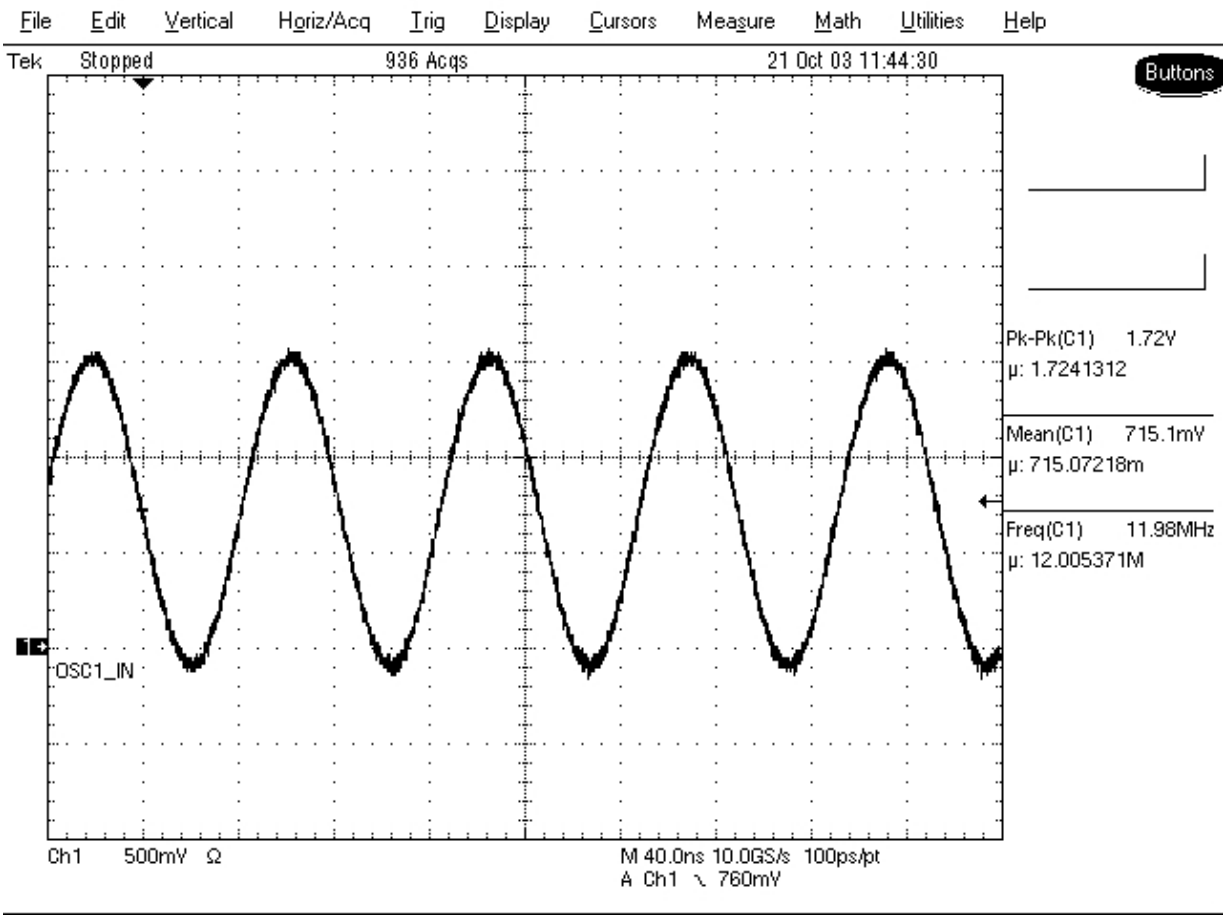

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Figure 42:12MHz APE system clock (measured from the OSC1_OUT pin of OMAP1510)

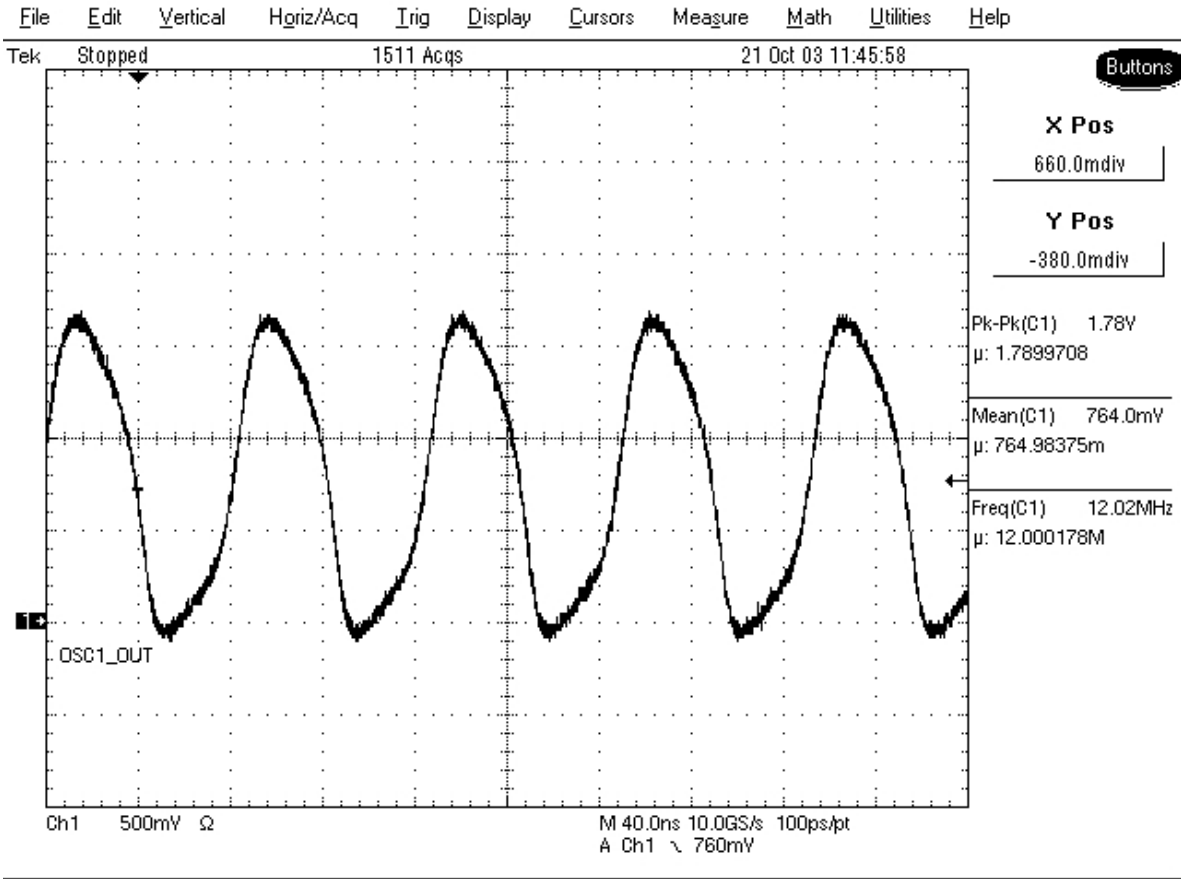

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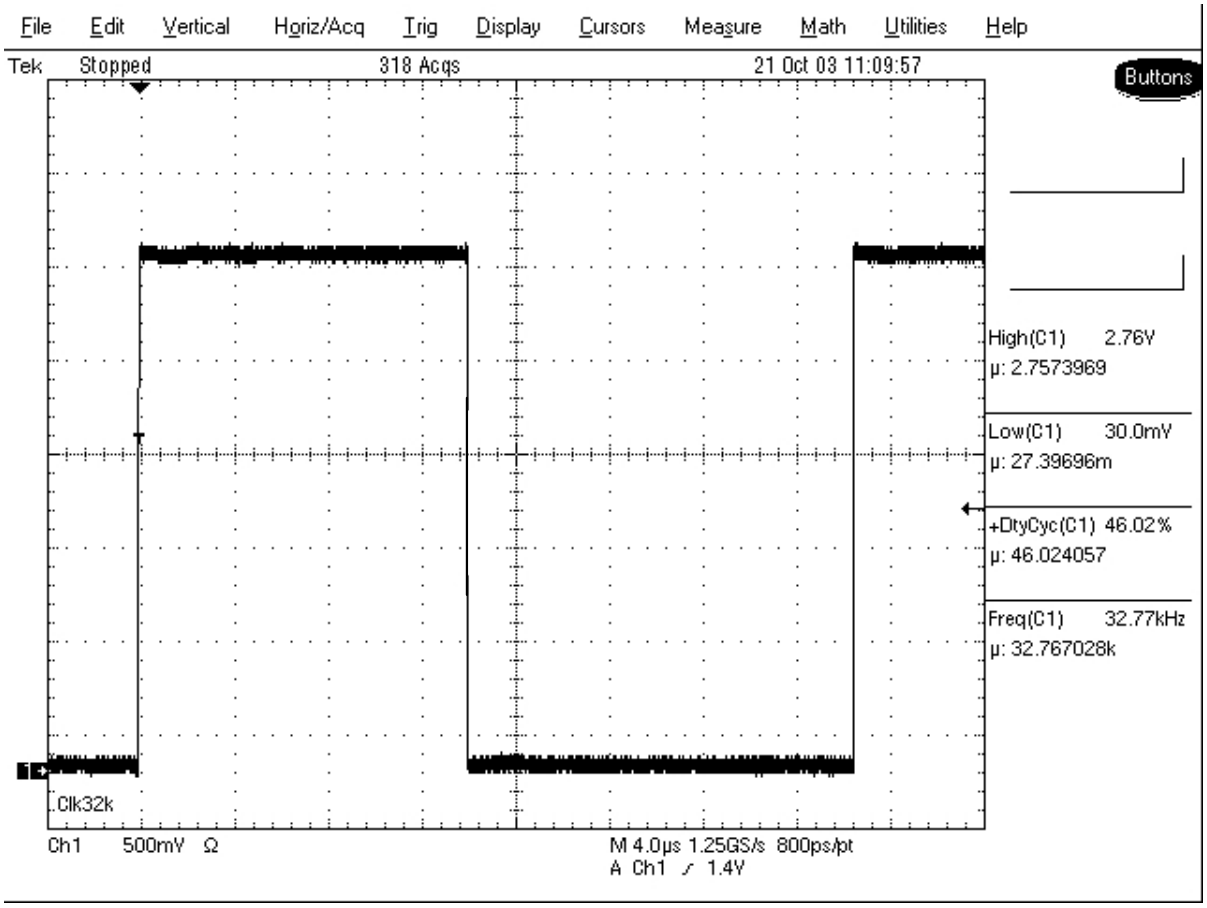
Figure 43:Clk32k



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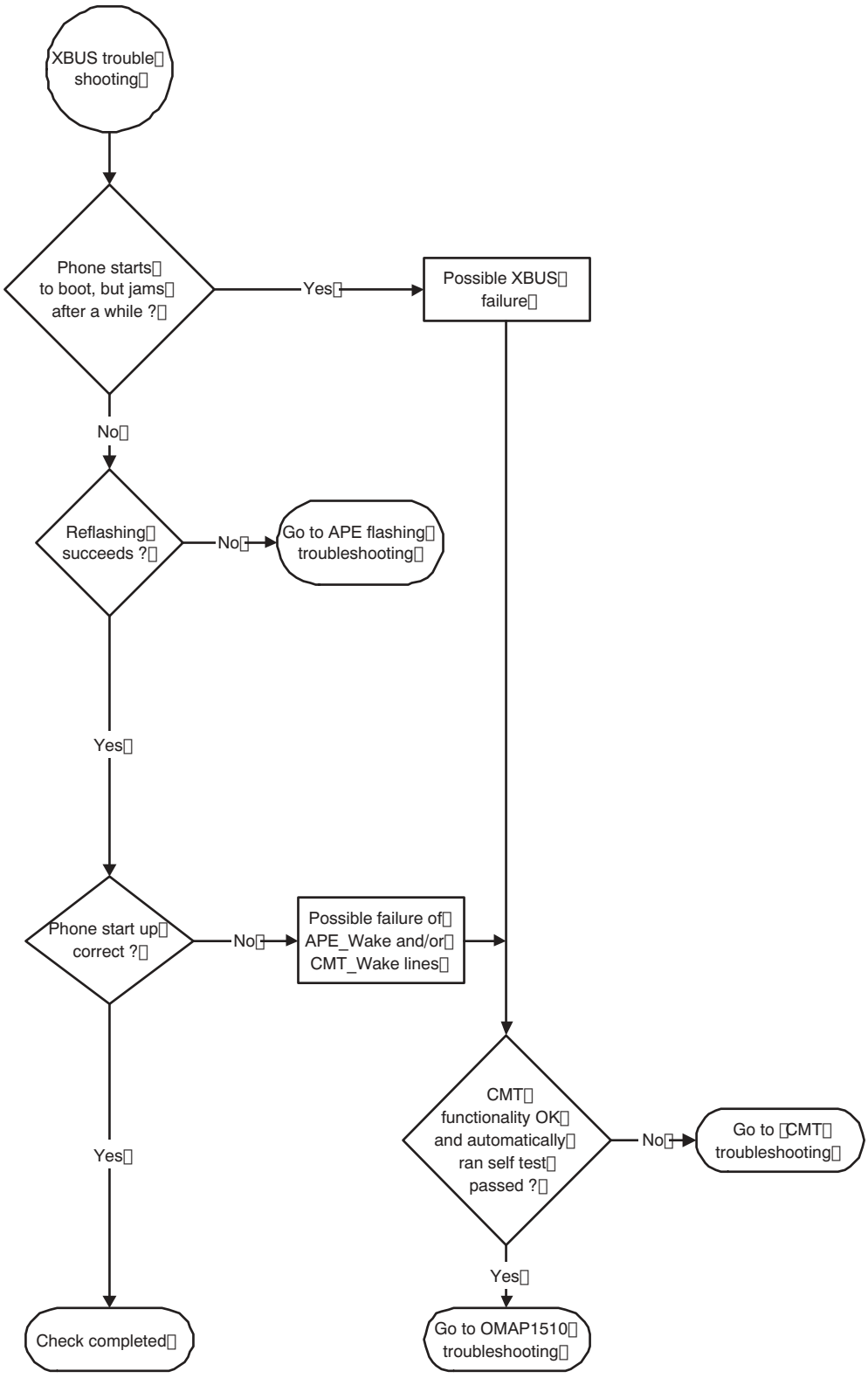
APE-CMT troubleshooting

APE-CMT interfaces

XBUS



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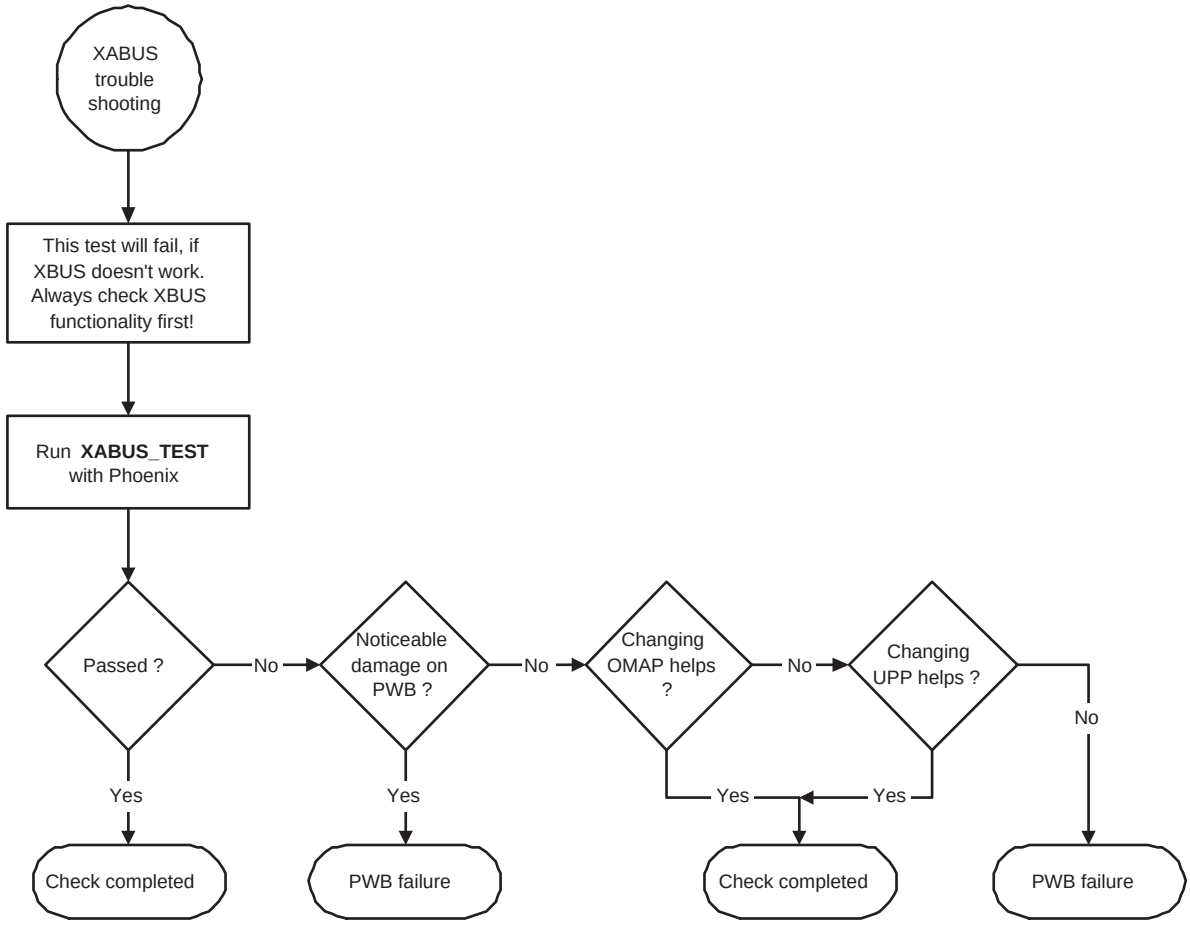
XABUS



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CMT serial interfaces troubleshooting

CBUS

CBUS is a three wire serial interface between the main baseband components. The bus consists of data, clock and bus_enable signals. In NHL-12 the bus is connected from UPP8M to ZOCUS and UEM. UPP8M takes care of controlling the traffic on the bus. If needed, CBUS can also be controlled by DSP. The CBUS electrical interface consists of a clock pin (CBusClk), a serial data input/output pin (CBusDa) and an enable pin (CBusEnX).

The transmission protocol used on CBUS is simple. One frame consists of an address byte, read/write flag (write = low) and 1 to 32 data bits (MSB first). Actually, the address byte is a combination of a 3-bit device address and a 5-bit register address. UPP writes data to and reads data from CBUS at the falling edge of CBusClk, while the slave device (UEM) uses the rising edges for both operations.

If you are able to get the phone to boot up and can reach Phoenix BB self tests, it is possible to test the functionality of each component attached to Cbus.

Use:

- ST_CURRENT_GAUGE_IF TEST
- ST_UEM_CBUS_IF_TEST to test UEM Cbus interface

If an error is found while testing any of the above components, you should replace the failing component.

FBUS

FBUS is a two wire Rx and Tx interface between the UPP and flash/test interface. The bus goes through the UEM which adjusts the voltage levels to suit UPP8M. The interface voltage level on the phone flash/test pad pattern is 2.78V and on the UPP8M end it is 1.8V. The functionality of this interface should not affect the device boot in NORMAL, LOCAL or TEST modes. Phoenix tests can be performed through MBUS interface in the case of a failure in FBUS interface. Flashing is not possible if there is a problem with FBUS.

MBUS

MBUS is a two wire Rx and Tx interface between the UPP and UEM. From the UEM, the MBUS interface continues to flash/test interface as a one wire interface. The UEM also adjusts the voltage levels. The interface voltage level on the phone flash/test pad pattern is 2.78V and on the UPP8M end it is 1.8V. MBUS traffic between the UPP8M and UEM can be tested with PHOENIX (ST_MBUS_RX_TX_LOOP_TEST). Flashing is not possible, if there is a problem with MBUS.

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USB troubleshooting

Figure 44:USB troubleshooting (1/2)

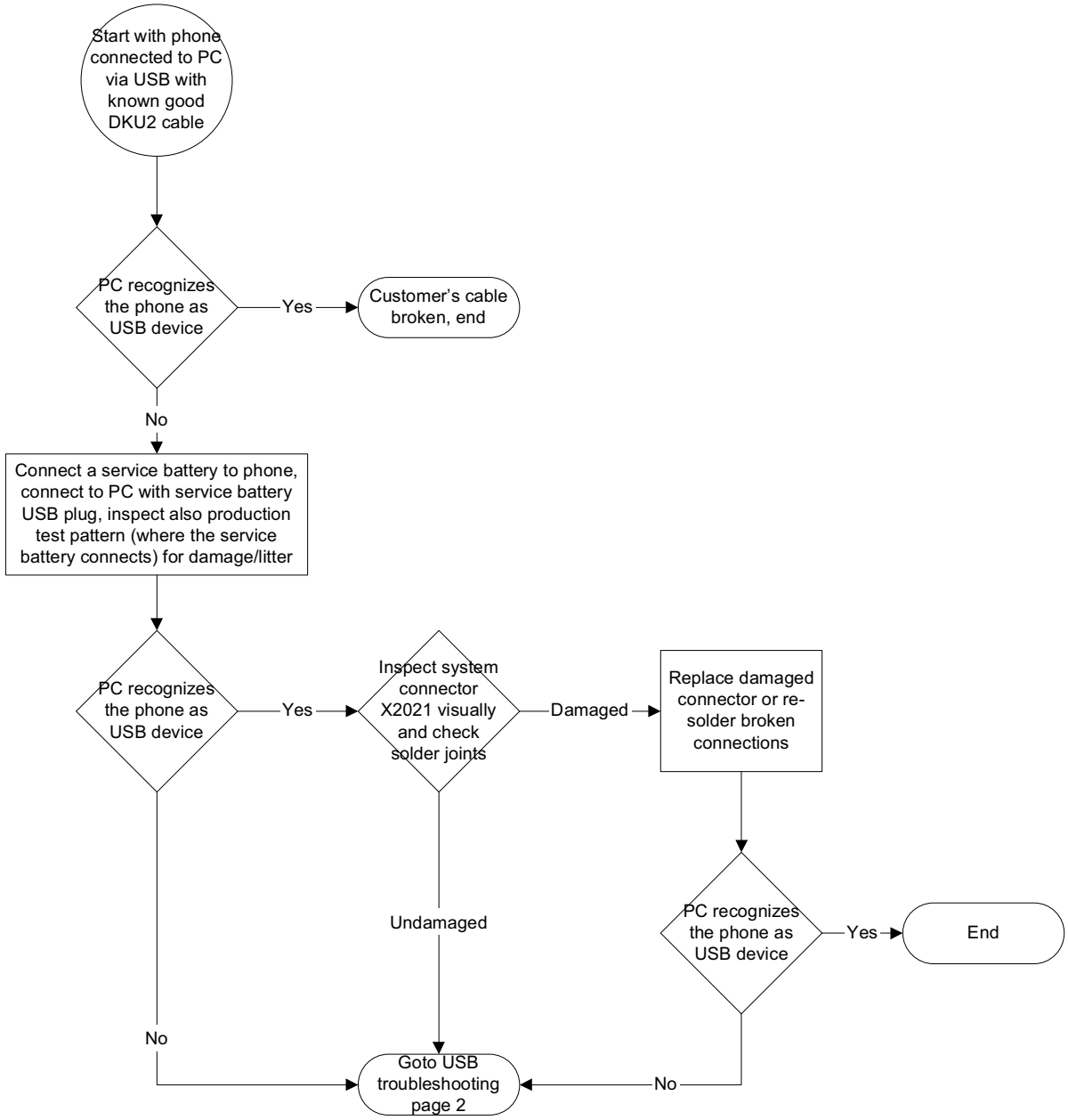
Start with phone connected to PC via USB with known good DKU2 cable
PC recognizes the phone as USB device
Yes
Customer's cable broken, end
No
Connect a service battery to phone, connect to PC with service battery USB plug, inspect also production test pattern (where the service battery connects) for damage/litter
PC recognizes the phone as USB device
Yes
Inspect system connector X2021 visually and check solder joints
Damaged
Replace damaged connector or re-solder broken connections
Undamaged
PC recognizes the phone as USB device
Yes
End
No
Goto USB troubleshooting page 2
No

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Figure 45:USB troubleshooting (2/2)

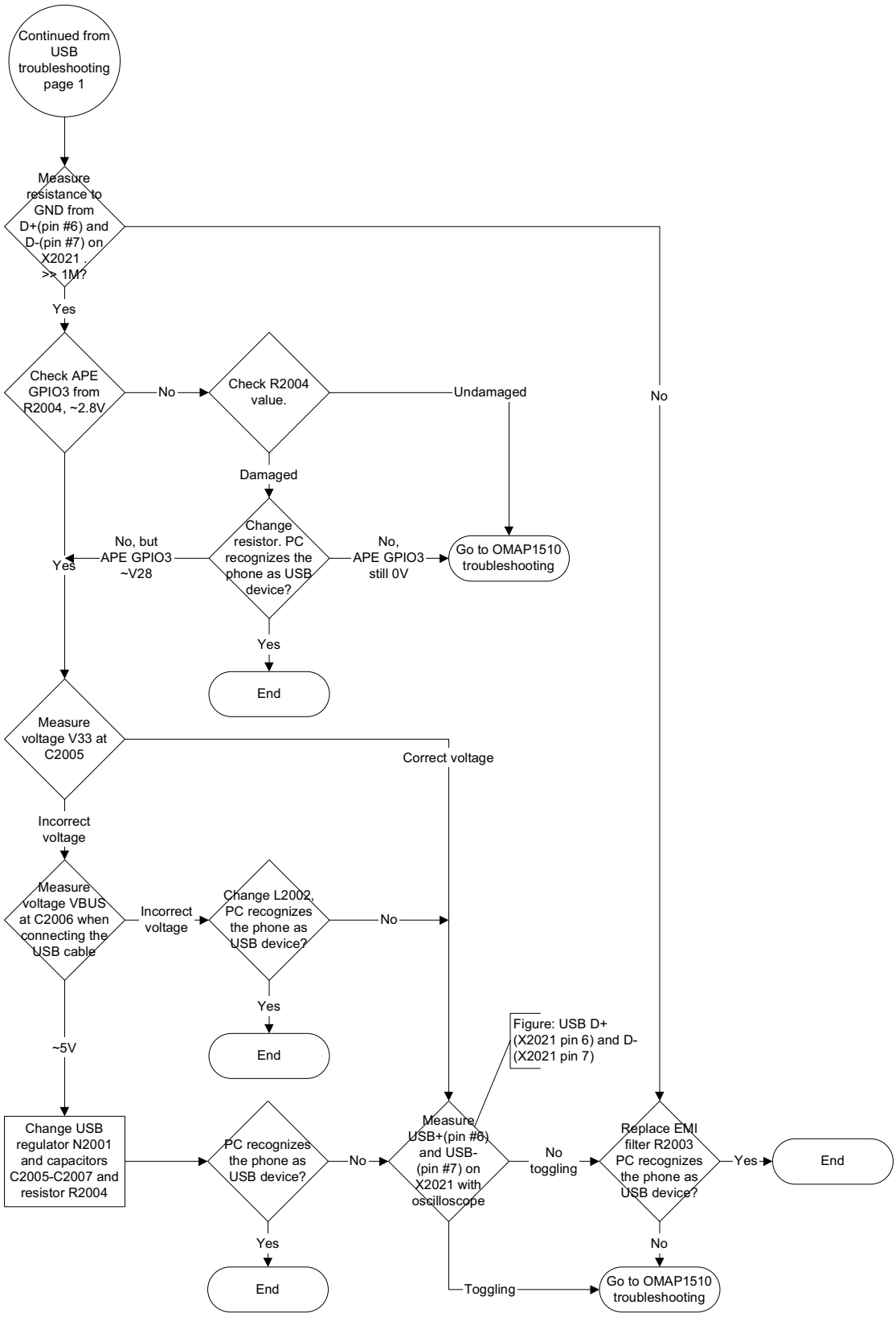

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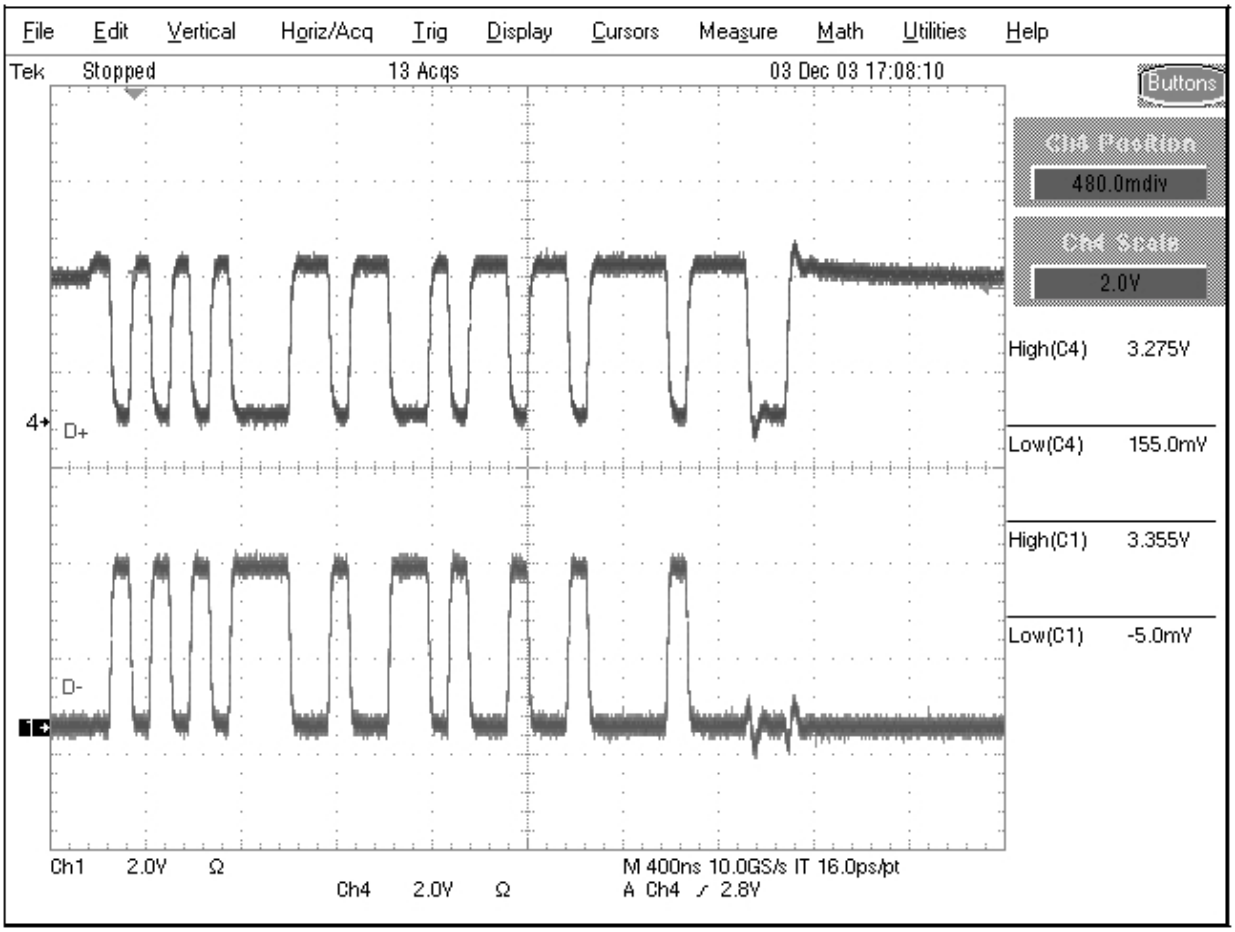
Figure 46:USB D+ (X2021 pin 6) and D- (X2021 pin 7)



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IrDa interface troubleshooting

Figure 47: IrDa interface troubleshooting (1/2)

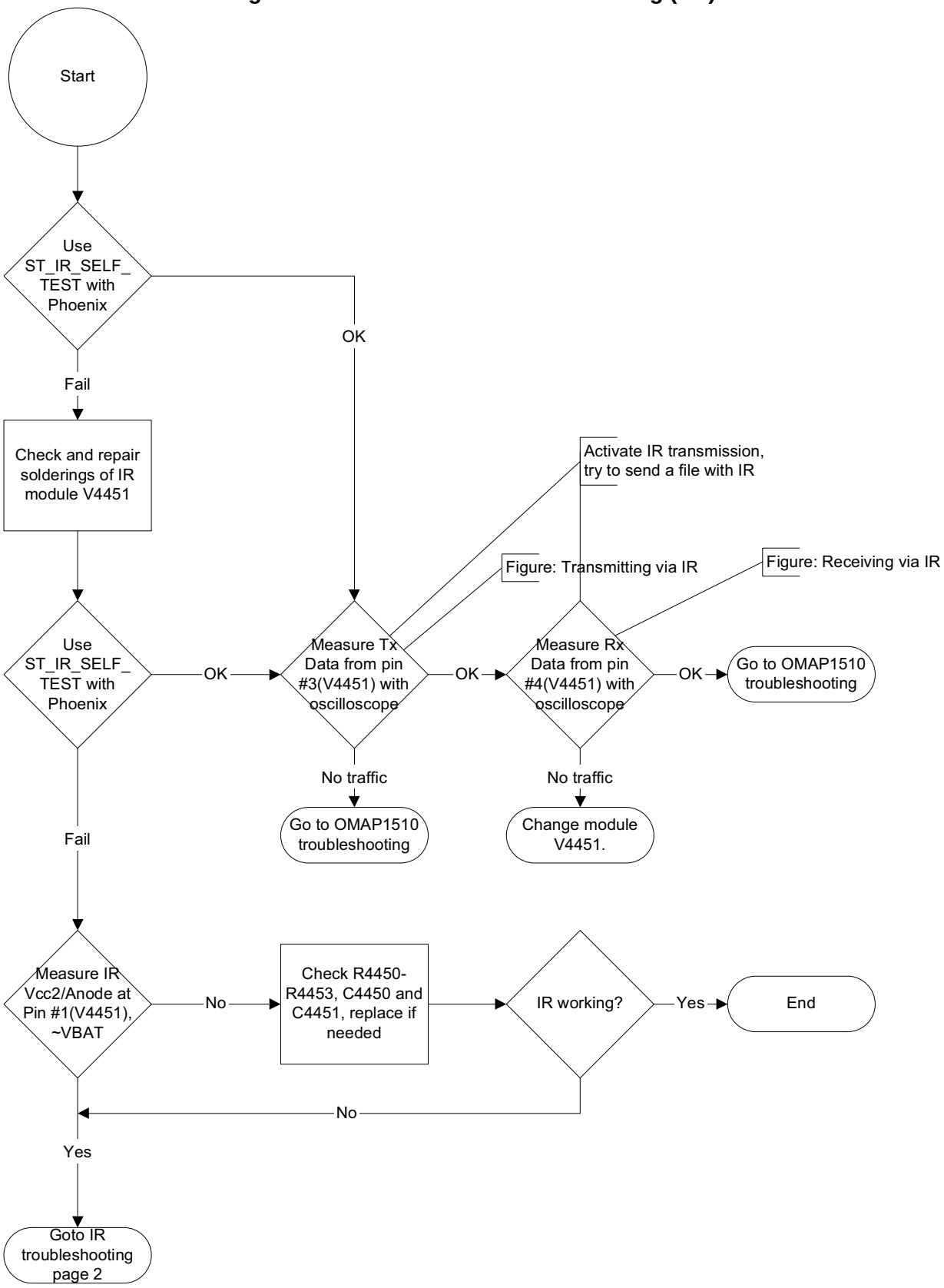

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Figure 48:IrDa interface troubleshooting (2/2)

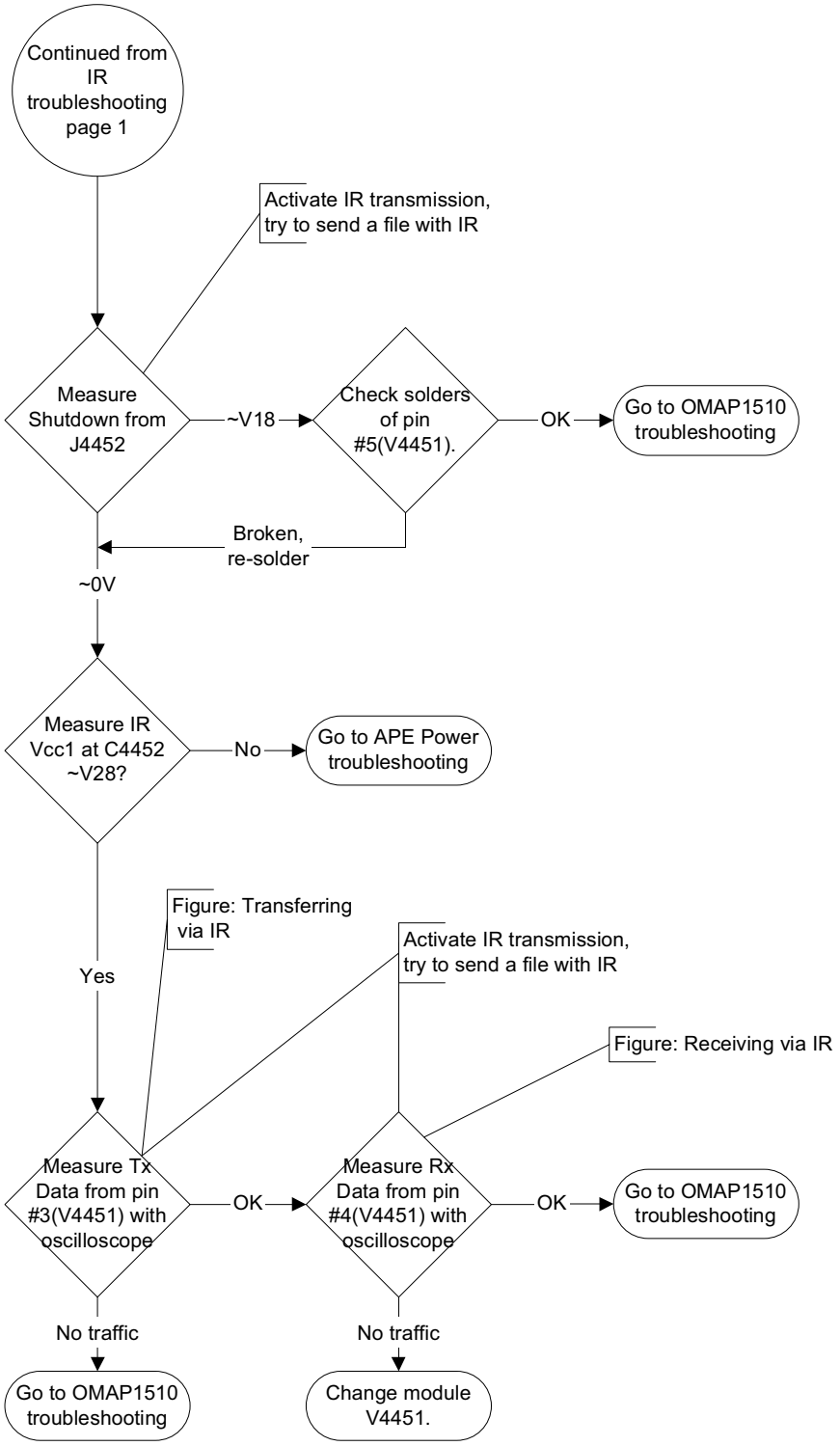

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Figure 49:Transferring via IR

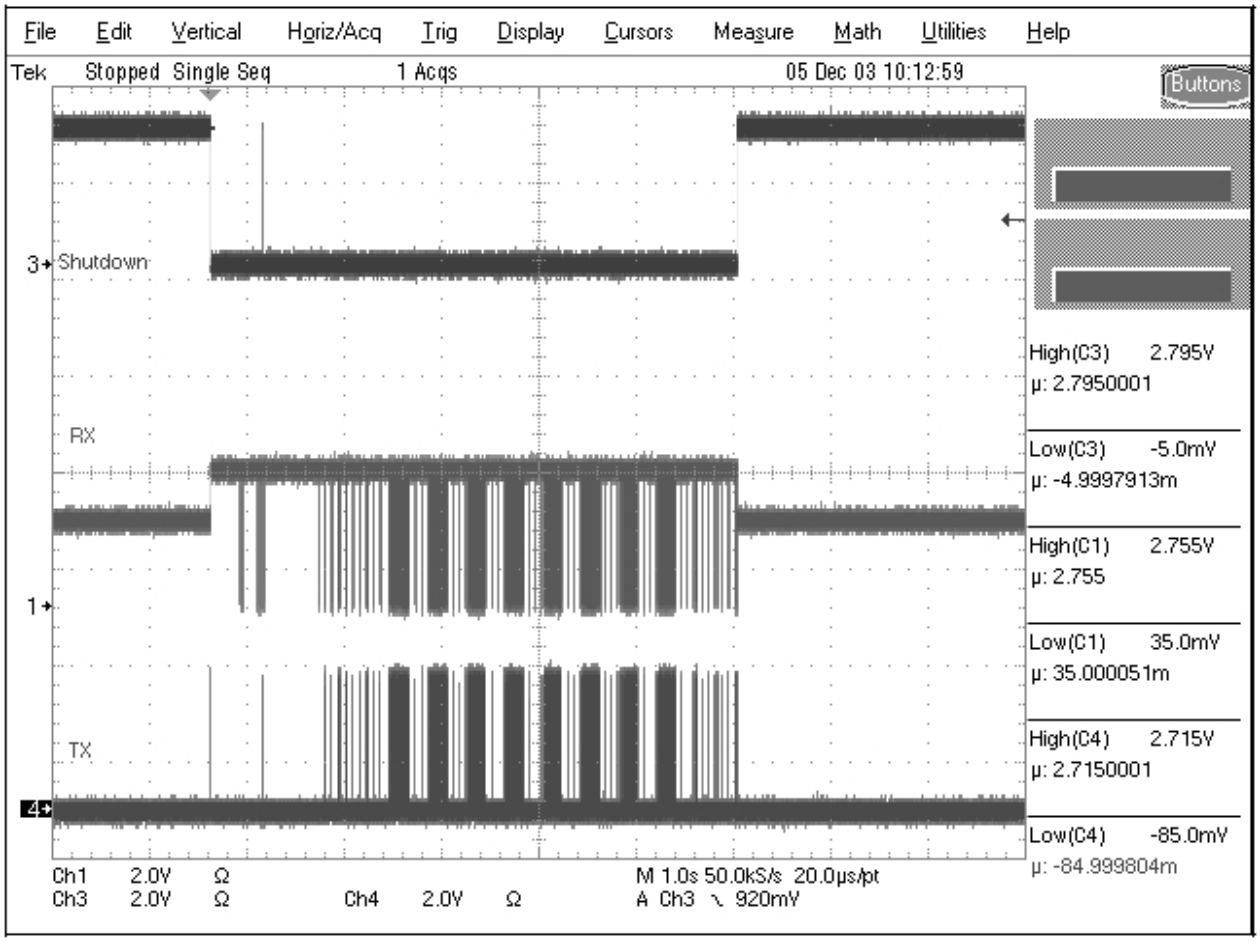

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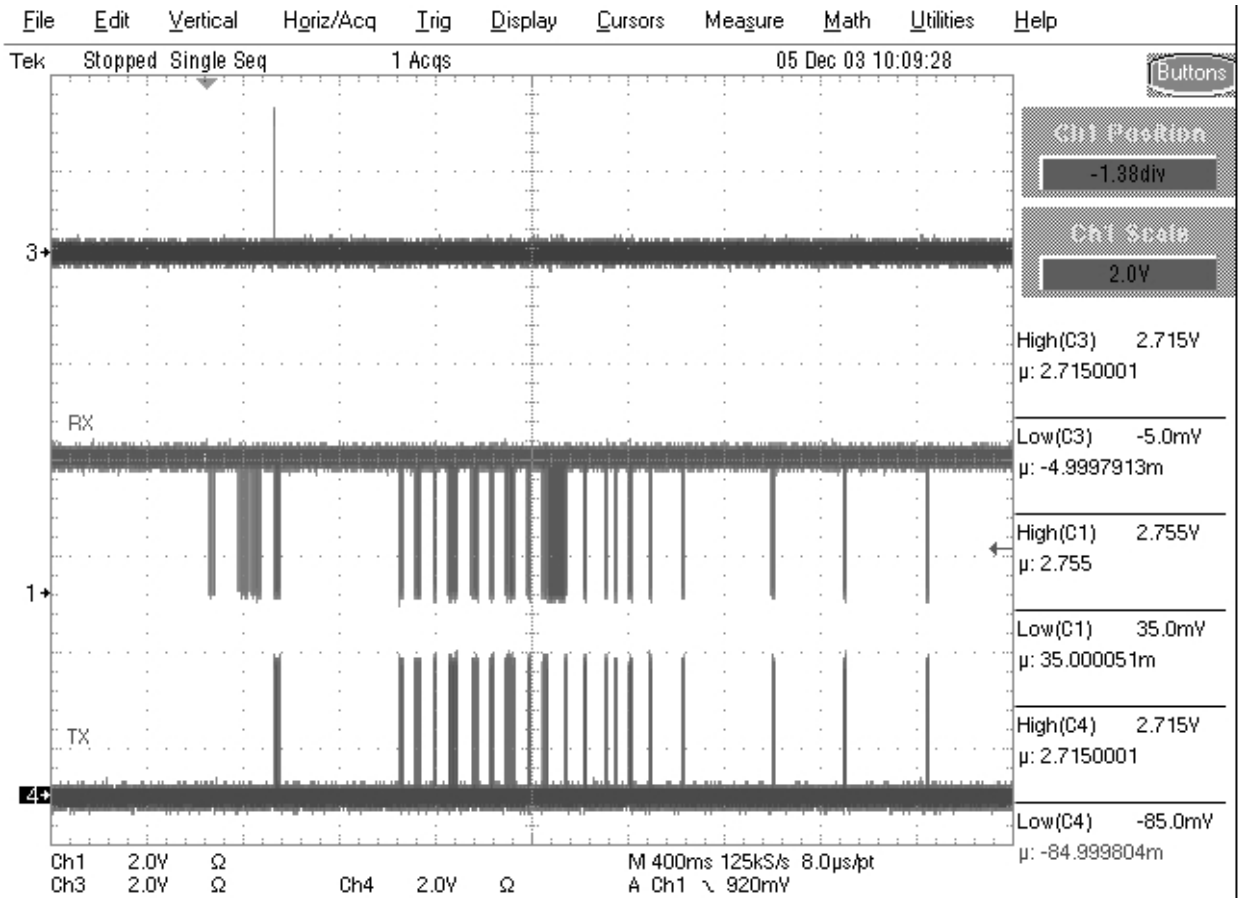
Figure 50:Receiving via IR



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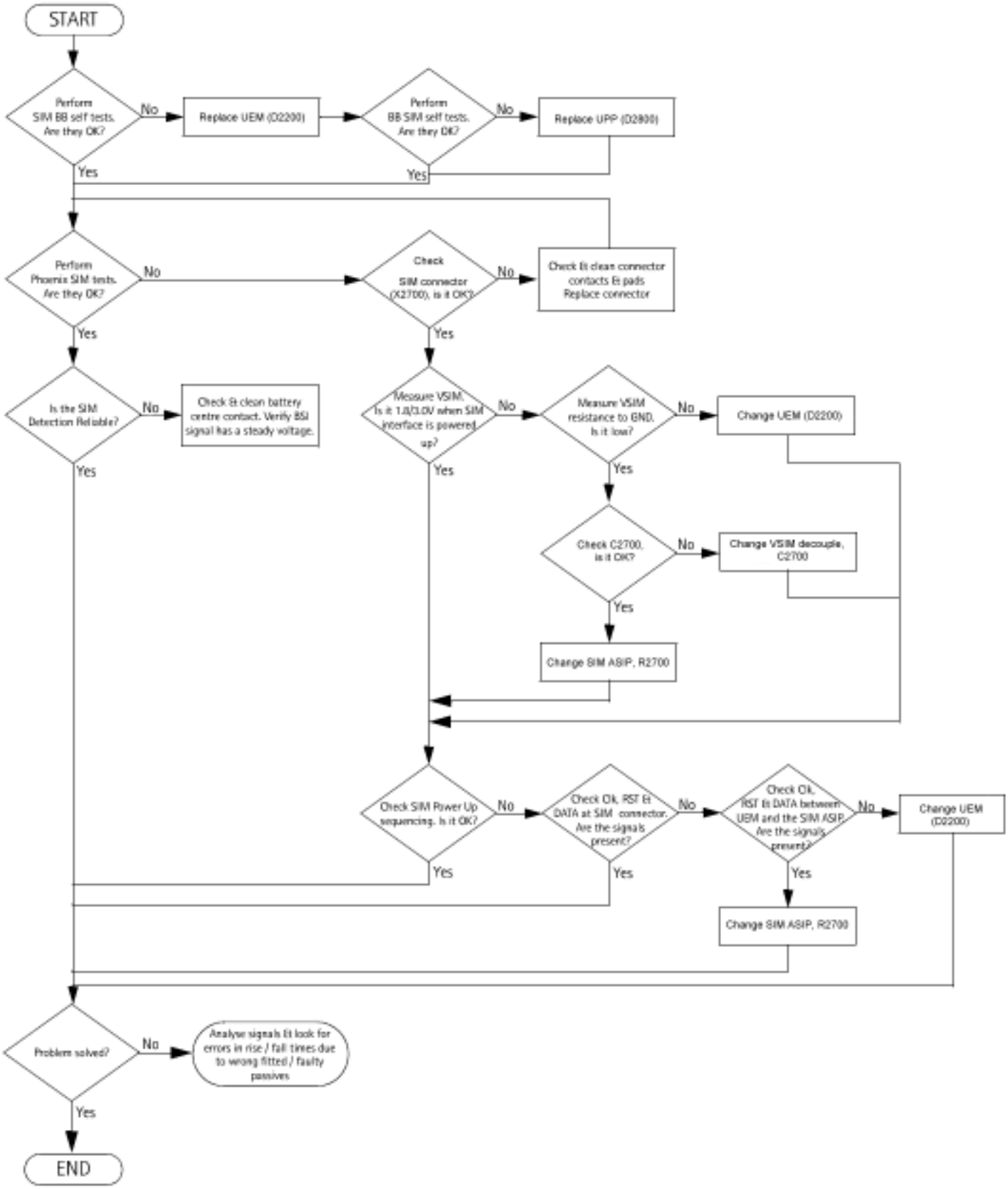
SIM card error



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UI failure

Display blank

If a part of the image is missing, replace the display. If there is no image at all or the image is otherwise corrupted, reflash the phone. If this does not help, follow the paths below.

Figure 51:Display blank (1/2)

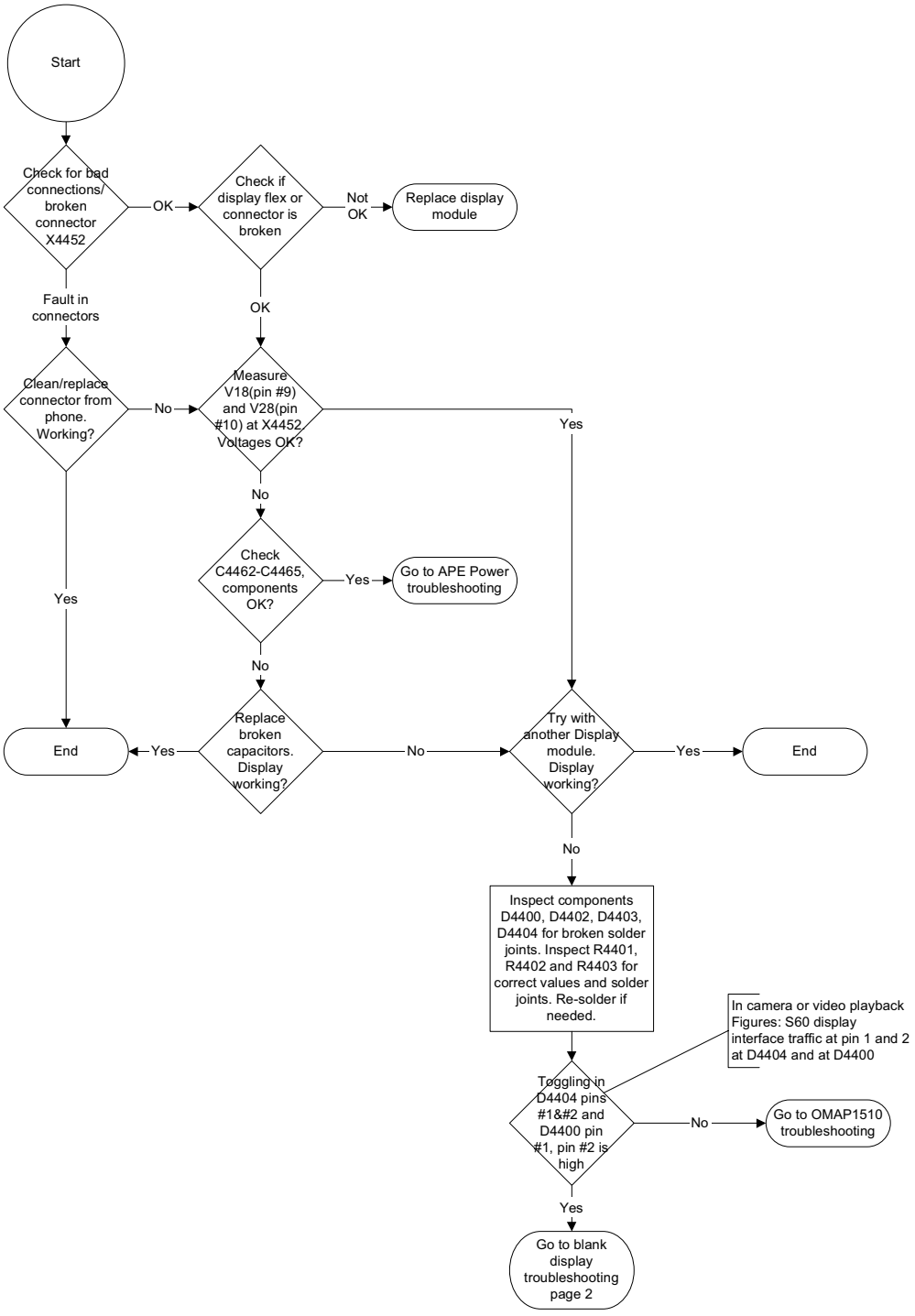
Start
Check for bad connections/ broken connector X4452
OK
Check if display flex or connector is broken
Not OK
Replace display module
Fault in connectors
OK
Clean/replace connector from phone. Working?
No
Measure V18(pin #9) and V28(pin #10) at X4452. Voltages OK?
Yes
No
Check C4462-C4465, components OK?
Yes
Go to APE Power troubleshooting
Yes
No
End
Yes
Replace broken capacitors. Display working?
No
Try with another Display module. Display working?
Yes
End
No
Inspect components D4400, D4402, D4403, D4404 for broken solder joints. Inspect R4401, R4402 and R4403 for correct values and solder joints. Re-solder if needed.
In camera or video playback Figures: S60 display interface traffic at pin 1 and 2 at D4404 and at D4400
Toggling in D4404 pins #1&#2 and D4400 pin #1, pin #2 is high
No
Go to OMAP1510 troubleshooting
Yes
Go to blank display troubleshooting page 2

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Figure 52:Display blank (2/2)

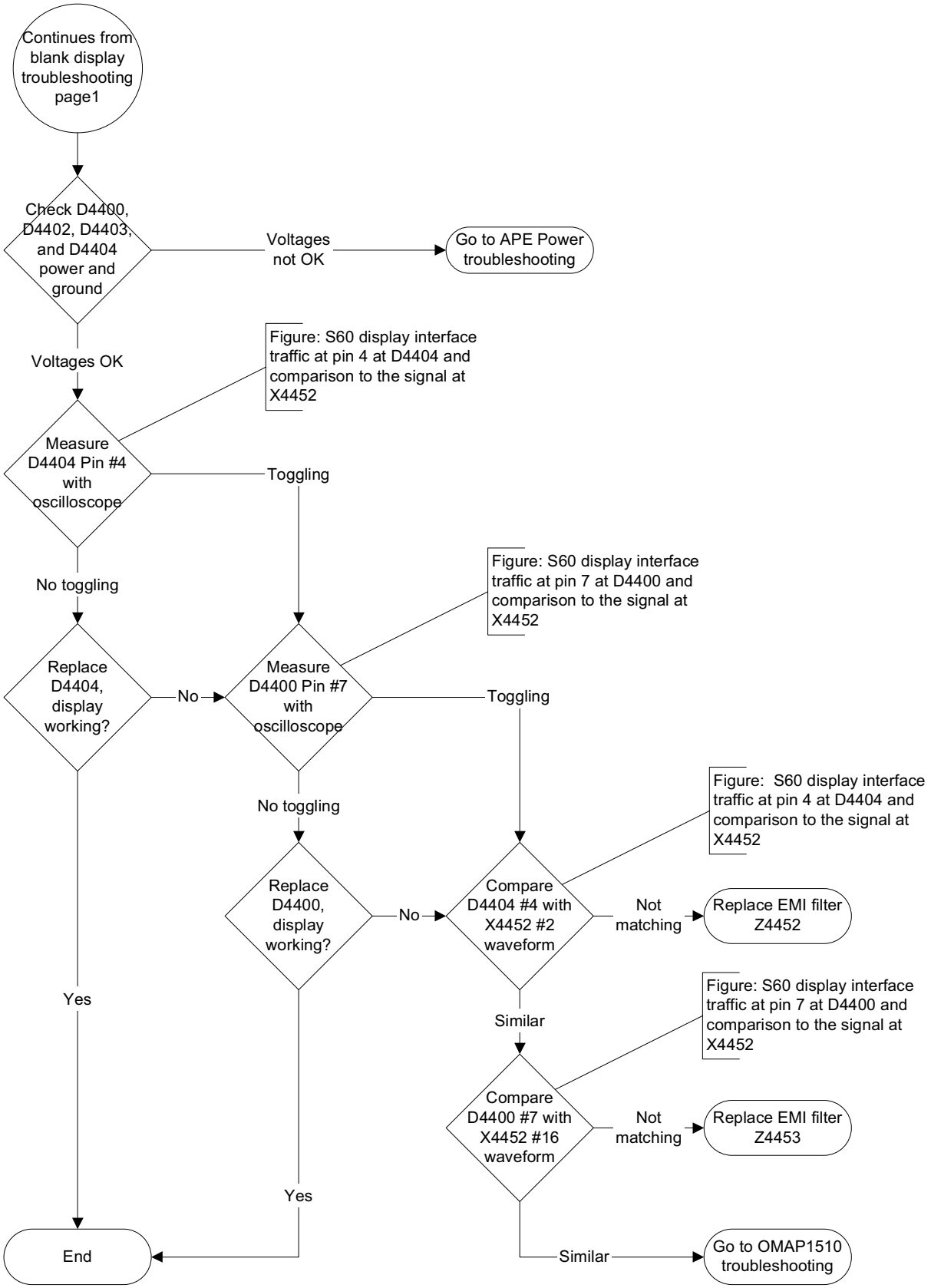
Continues from blank display troubleshooting page1
Check D4400, D4402, D4403, and D4404 power and ground
Voltages not OK
Go to APE Power troubleshooting
Voltages OK
Figure: S60 display interface traffic at pin 4 at D4404 and comparison to the signal at X4452
Measure D4404 Pin #4 with oscilloscope
Toggling
No toggling
Figure: S60 display interface traffic at pin 7 at D4400 and comparison to the signal at X4452
Replace D4404, display working?
No
Measure D4400 Pin #7 with oscilloscope
Toggling
No toggling
Figure: S60 display interface traffic at pin 4 at D4404 and comparison to the signal at X4452
Replace D4400, display working?
No
Compare D4404 #4 with X4452 #2 waveform
Not matching
Replace EMI filter Z4452
Yes
Similar
Figure: S60 display interface traffic at pin 7 at D4400 and comparison to the signal at X4452
Compare D4400 #7 with X4452 #16 waveform
Not matching
Replace EMI filter Z4453
Yes
End
Similar
Go to OMAP1510 troubleshooting

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Figure 53:S60 display interface traffic at pin 4 at D4404 and comparison to the signal at X4452

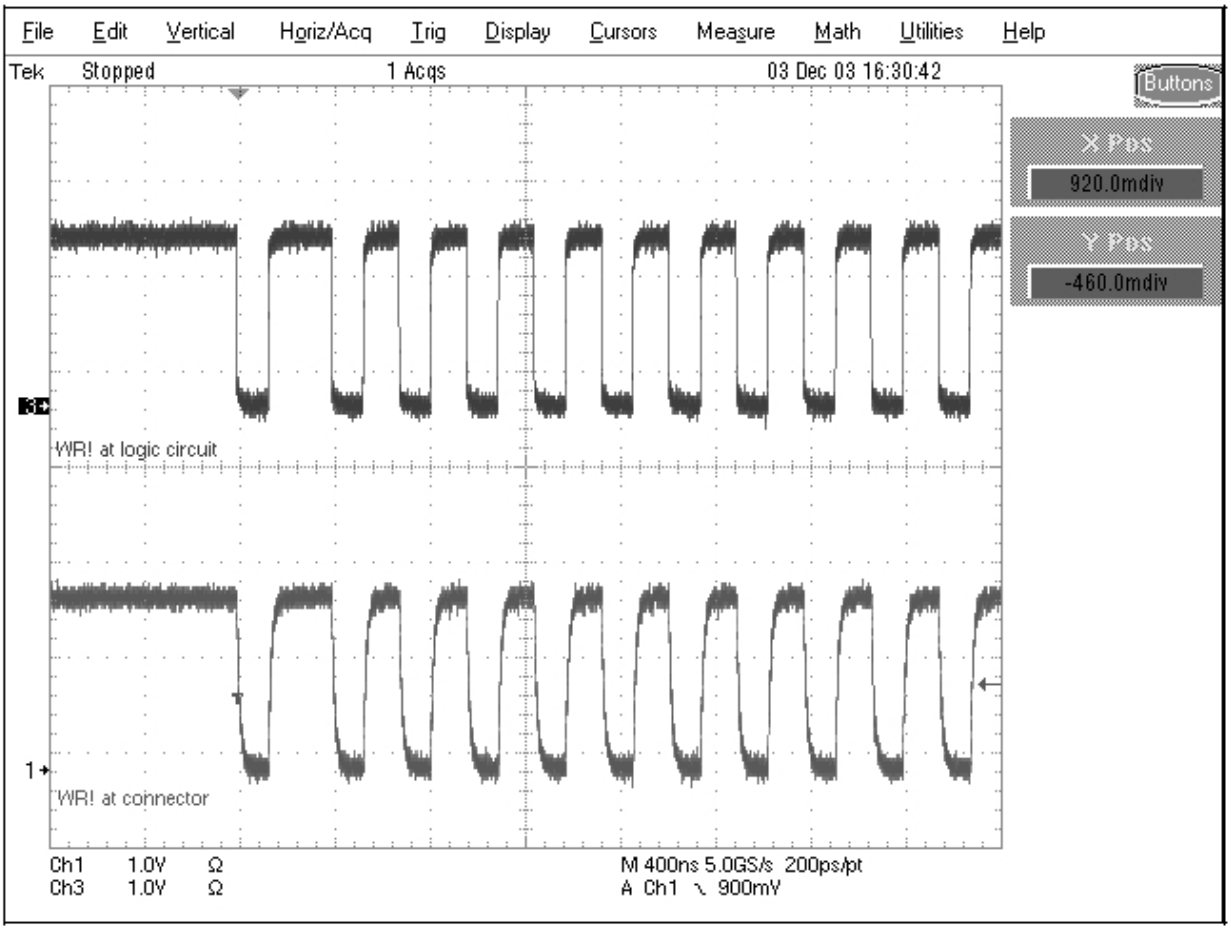

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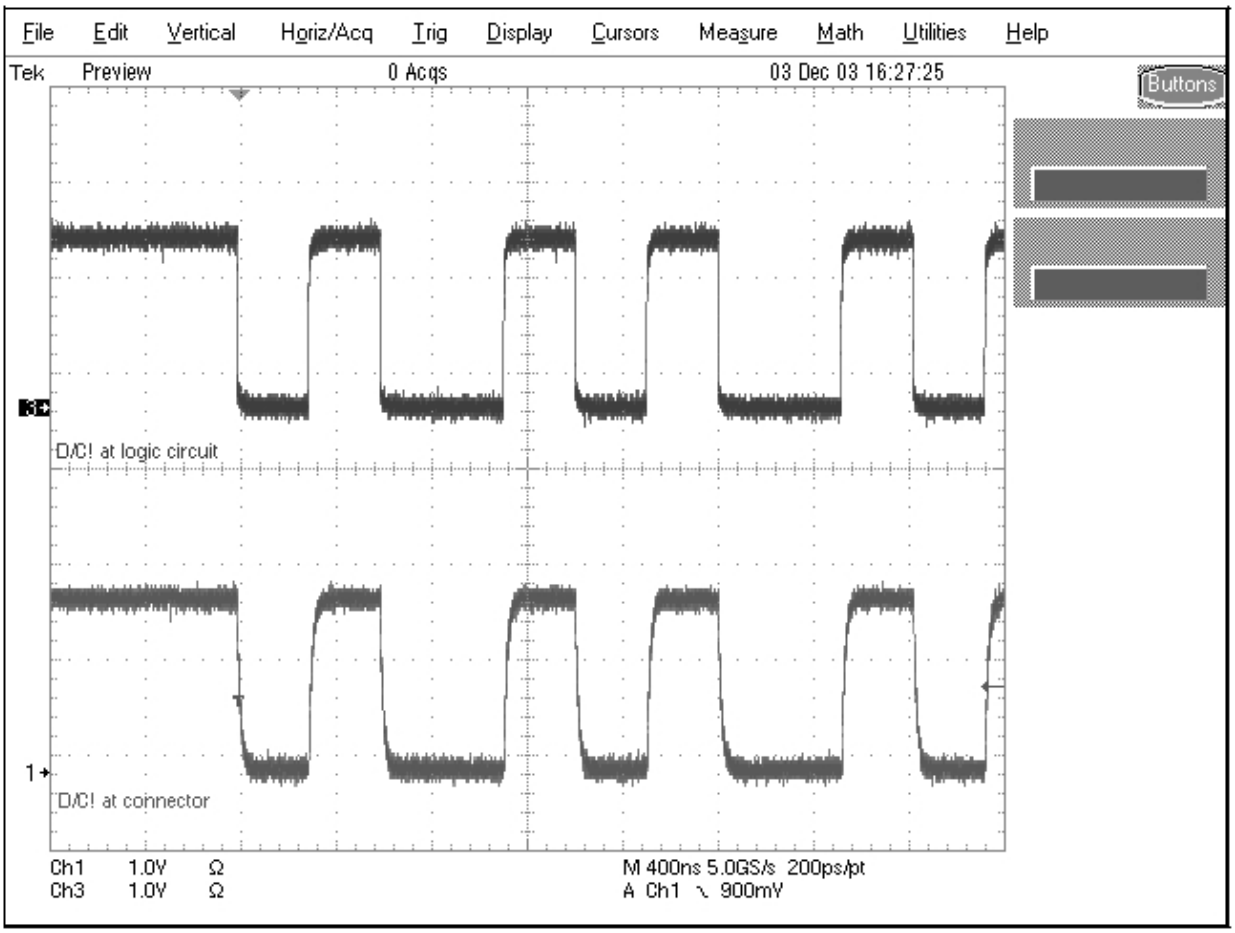
Figure 54:S60 display interface traffic at pin 7 at D4400 and comparison to the signal at X4452


File Edit Vertical Horiz/Acq Trig Display Cursors Measure Math Utilities Help
Tek Preview 0 Acqs 03 Dec 03 16:27:25
Buttons
D/C! at logic circuit
D/C! at connector
Ch1 1.0V Ω
Ch3 1.0V Ω
M 400ns 5.0GS/s 200ps/pt
A Ch1 ∖ 900mV

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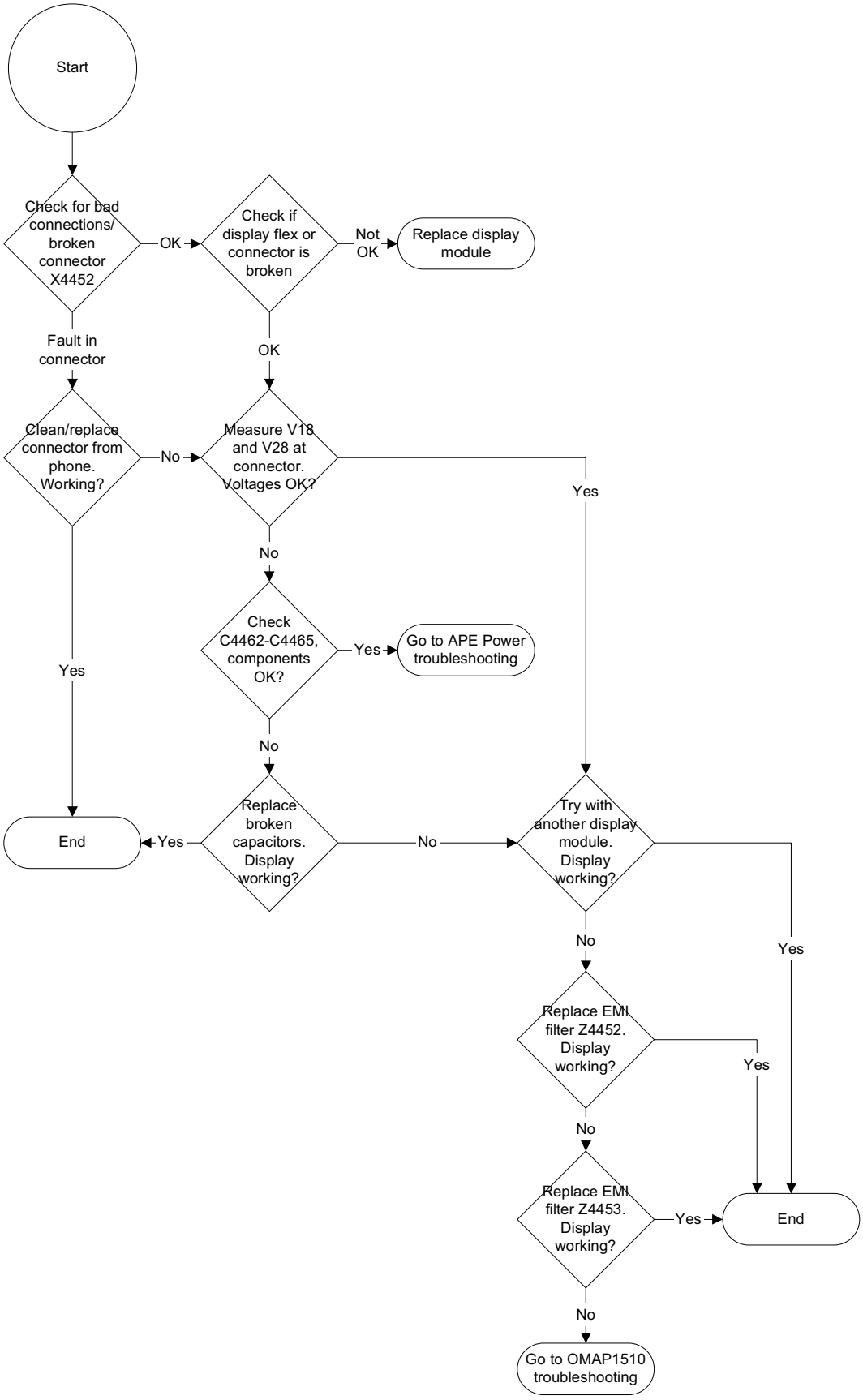
Display distorted



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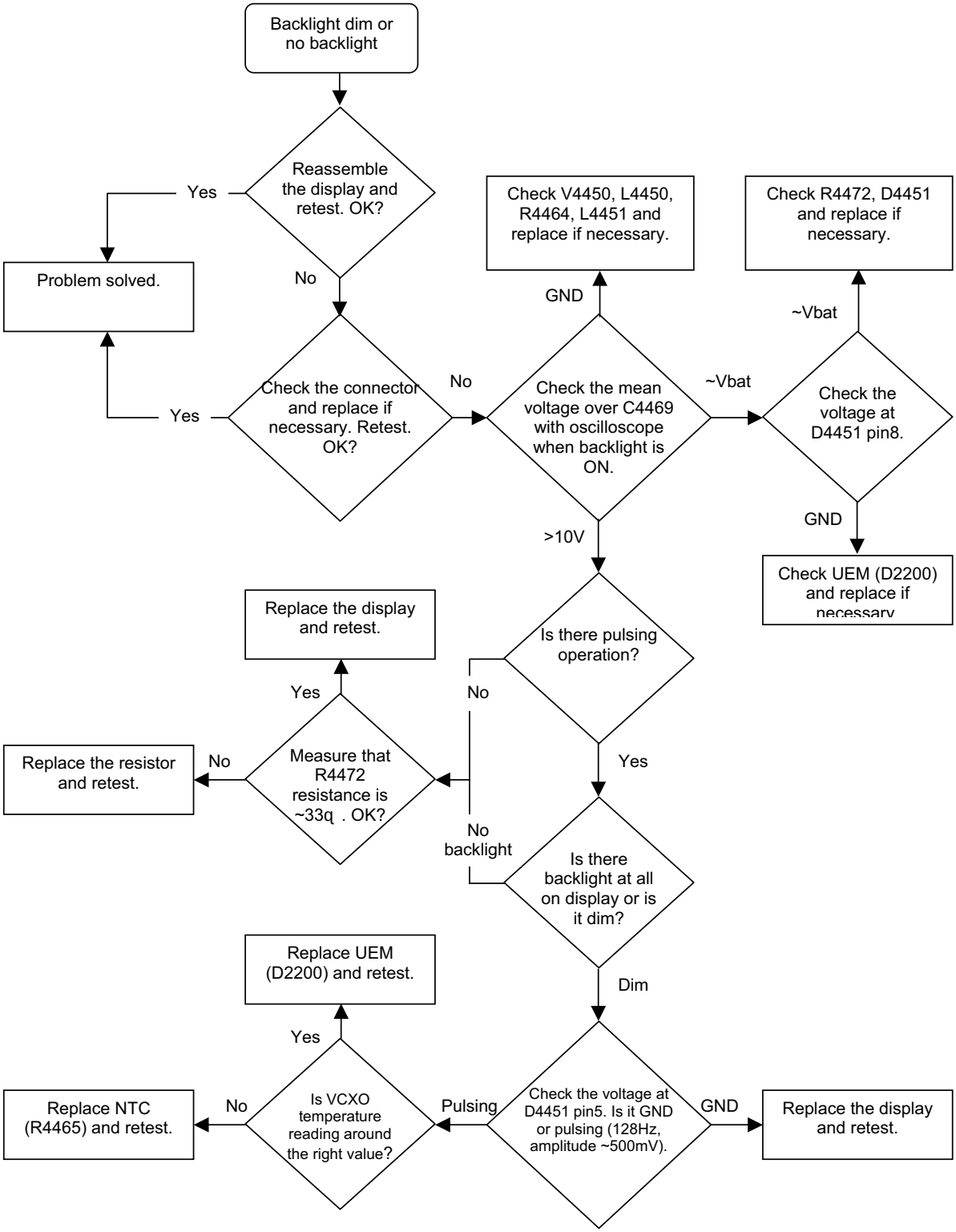
Display backlight dim or no backlight


Backlight dim or no backlight
Reassemble the display and retest. OK?
Yes
Problem solved.
No
Check the connector and replace if necessary. Retest. OK?
Yes
No
Check the mean voltage over C4469 with oscilloscope when backlight is ON.
GND
Check V4450, L4450, R4464, L4451 and replace if necessary.
~Vbat
Check R4472, D4451 and replace if necessary.
~Vbat
Check the voltage at D4451 pin8.
GND
Check UEM (D2200) and replace if necessary
>10V
Is there pulsing operation?
No
Yes
Is there backlight at all on display or is it dim?
No backlight
Dim
Check the voltage at D4451 pin5. Is it GND or pulsing (128Hz, amplitude ~500mV).
GND
Replace the display and retest.
Pulsing
Is VCXO temperature reading around the right value?
No
Replace NTC (R4465) and retest.
Yes
Replace UEM (D2200) and retest.
Measure that R4472 resistance is ~33q . OK?
No
Replace the resistor and retest.
Yes
Replace the display and retest.

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Keyboard backlight

There are two kinds of problems with the keyboard backlight. The backlight may be dim or there is no backlight at all. The following flowchart describes how these problems can be detected and solved.

Note! It is possible for one LED to be non-functional and all the other LEDs to be still working.

Figure 55:Keyboard backlight failure (1/2)

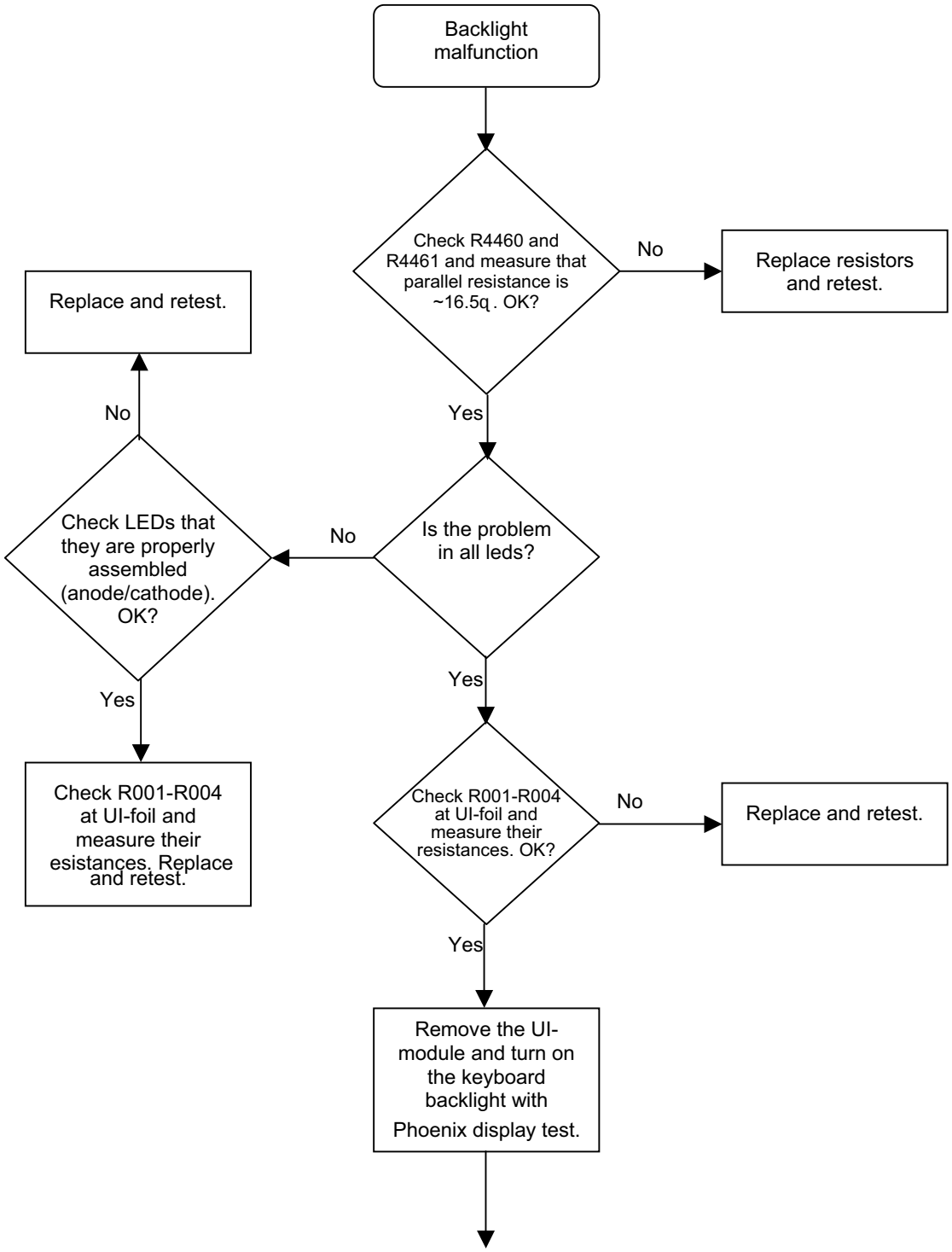
Backlight malfunction
Check R4460 and R4461 and measure that parallel resistance is ~16.5q . OK?
No
Replace resistors and retest.
Yes
Is the problem in all leds?
No
Check LEDs that they are properly assembled (anode/cathode). OK?
No
Replace and retest.
Yes
Check R001-R004 at UI-foil and measure their esistances. Replace and retest.
Yes
Check R001-R004 at UI-foil and measure their resistances. OK?
No
Replace and retest.
Yes
Remove the UI-module and turn on the keyboard backlight with Phoenix display test.

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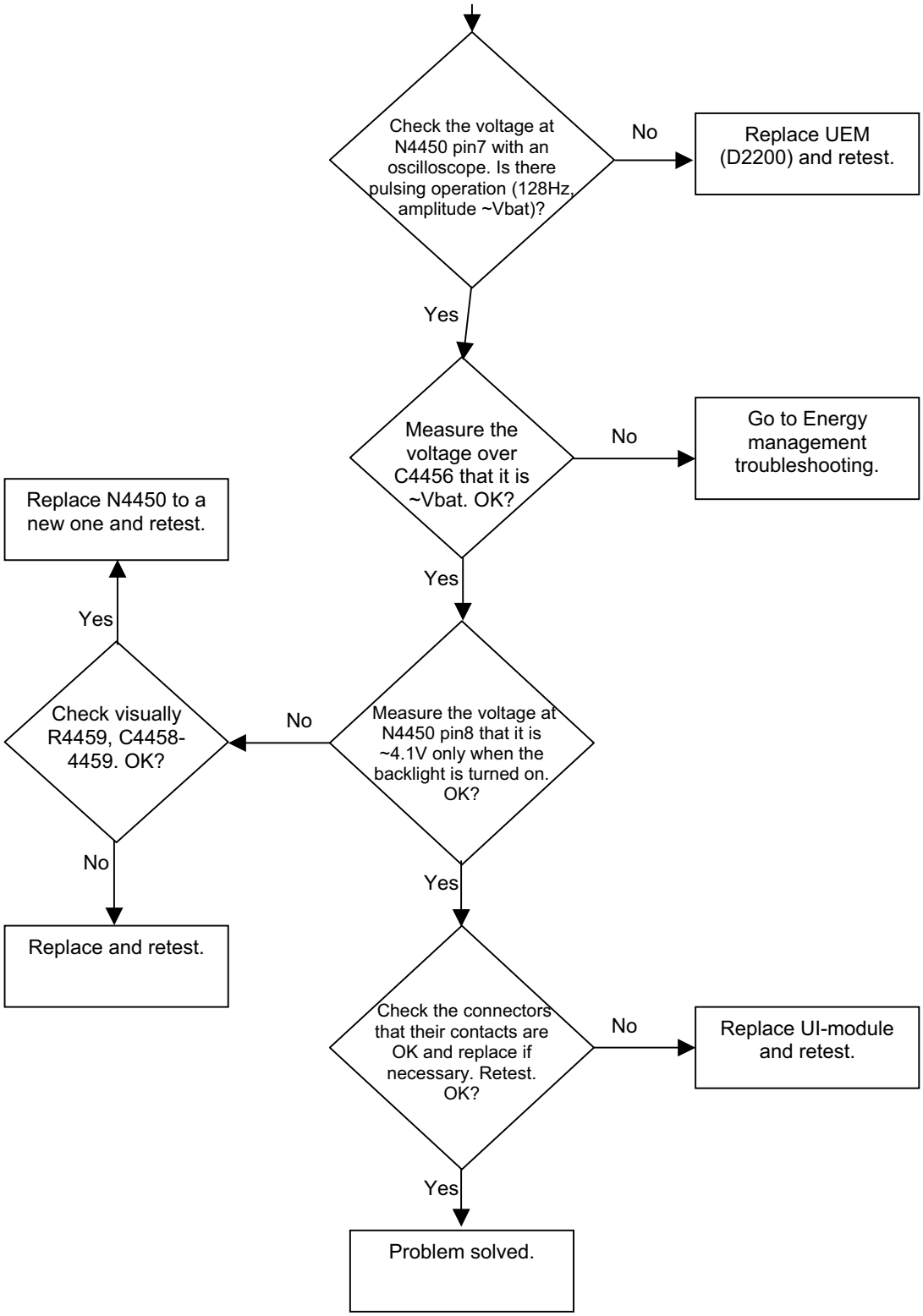
Figure 56:Keyboard backlight failure (2/2)


Check the voltage at N4450 pin7 with an oscilloscope. Is there pulsing operation (128Hz, amplitude ~Vbat)?
No
Replace UEM (D2200) and retest.
Yes
Measure the voltage over C4456 that it is ~Vbat. OK?
No
Go to Energy management troubleshooting.
Yes
Measure the voltage at N4450 pin8 that it is ~4.1V only when the backlight is turned on. OK?
No
Check visually R4459, C4458-4459. OK?
Yes
Replace N4450 to a new one and retest.
No
Replace and retest.
Yes
Check the connectors that their contacts are OK and replace if necessary. Retest. OK?
No
Replace UI-module and retest.
Yes
Problem solved.

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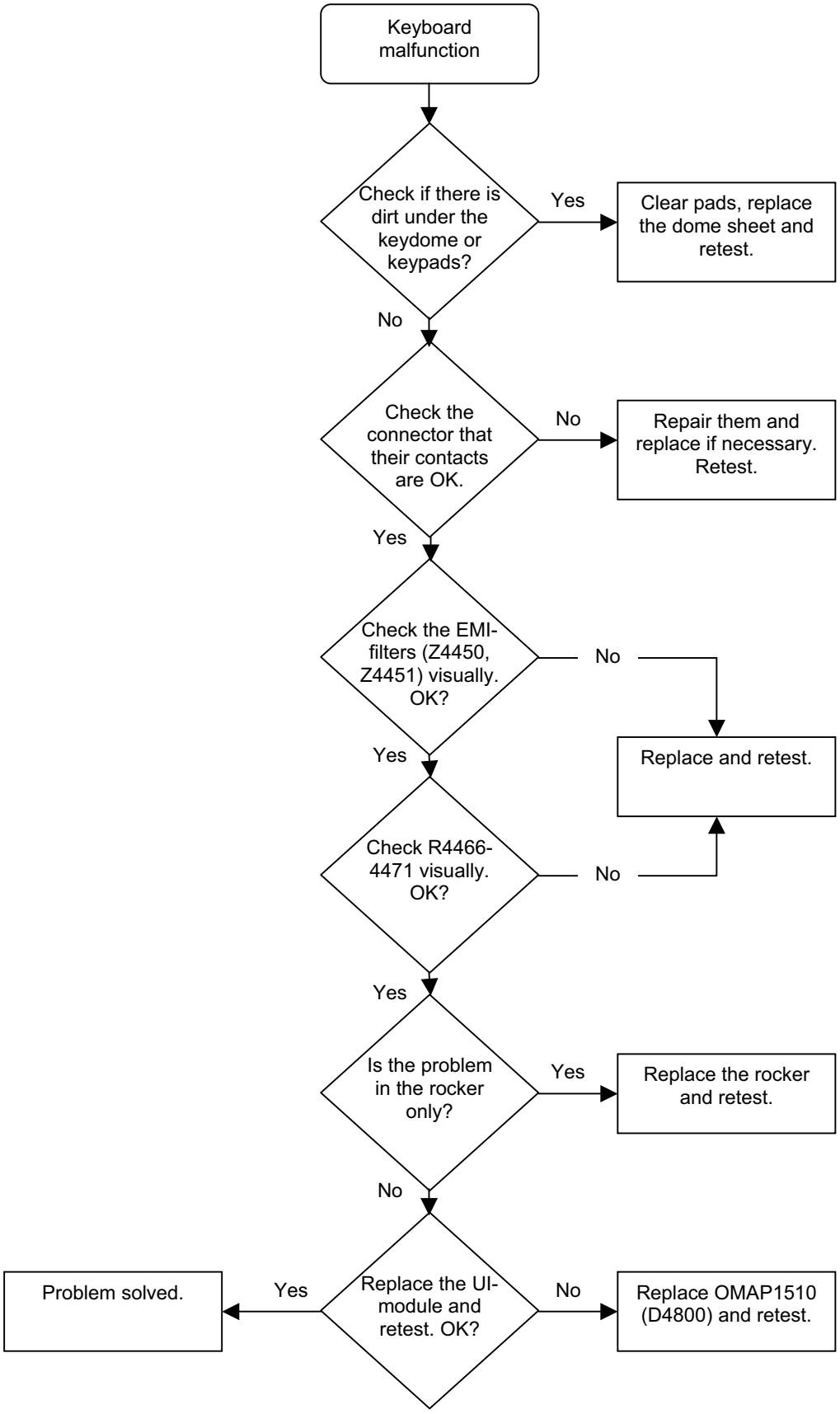
Keyboard malfunction



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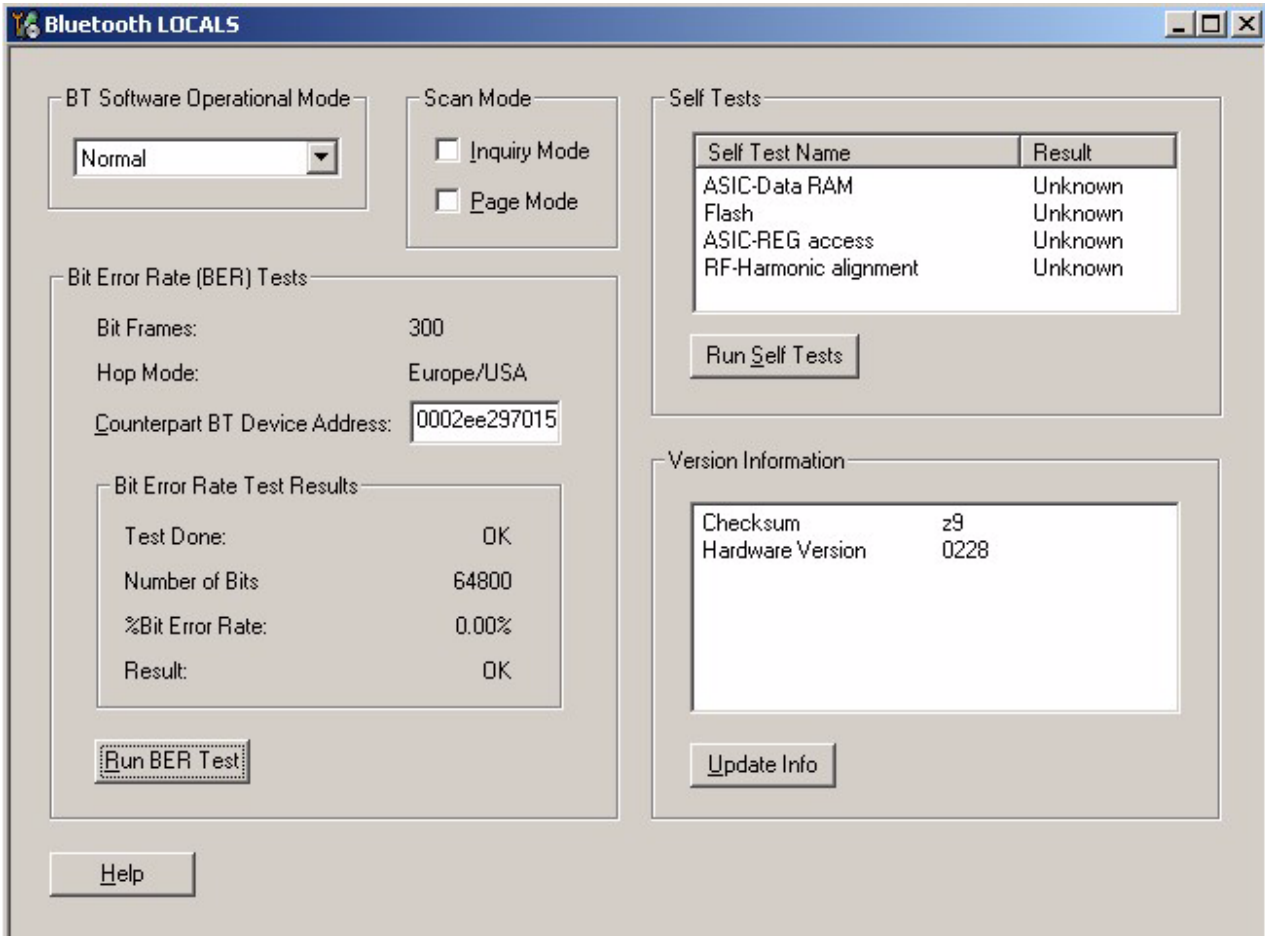
Bluetooth troubleshooting

Bluetooth settings for Phoenix

1. Connect phone to Phoenix in 'local' mode (from the Product menu, choose Choose Product).
2. From the Testing menu, choose Bluetooth LOCALS.

Figure 57:Bluetooth LOCALS window



3. Run BER test when JBT-9 box is close to the BT antenna.

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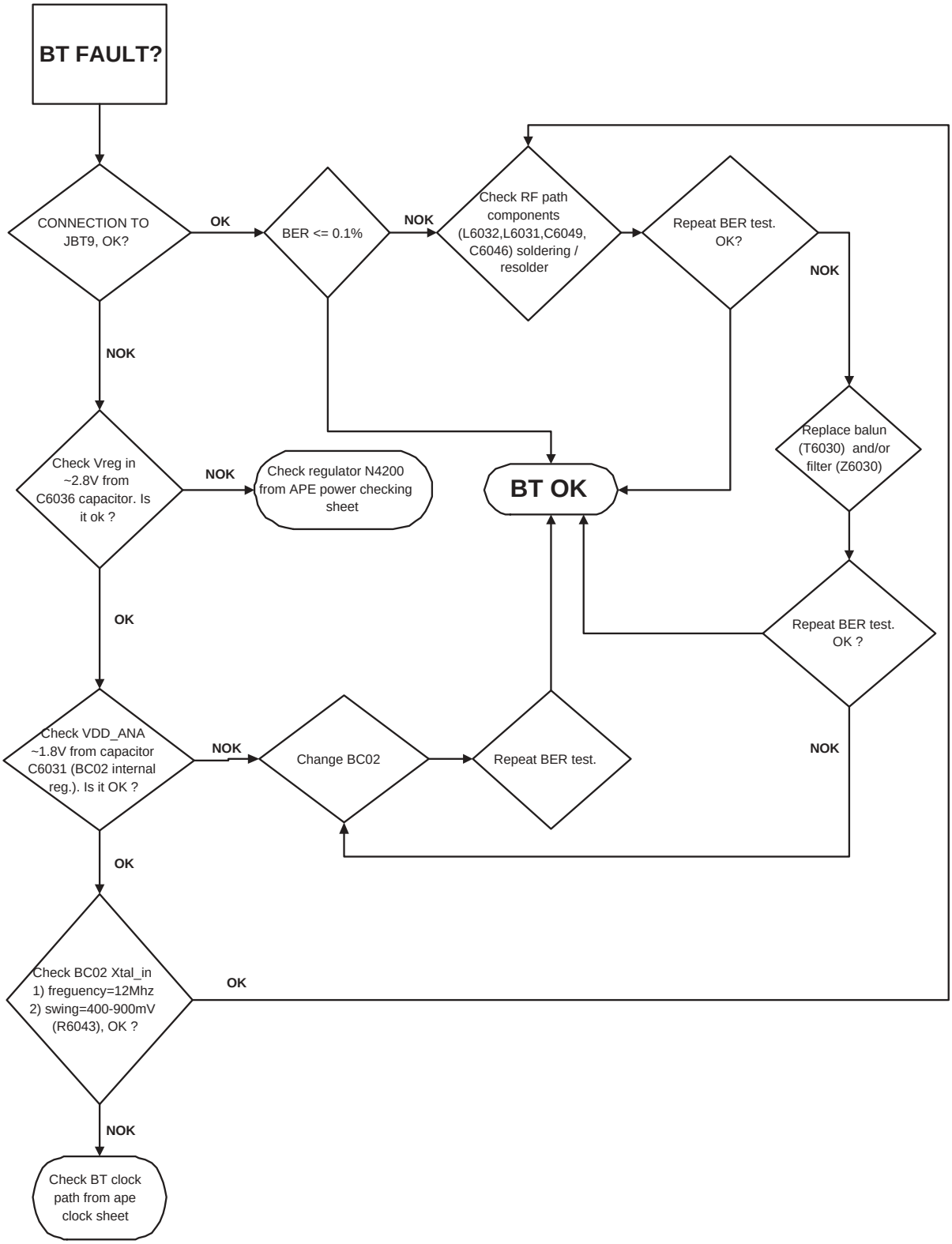
Bluetooth troubleshooting flowchart



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Multimedia card (MMC) troubleshooting

Figure 58:MMC troubleshooting (1/2)

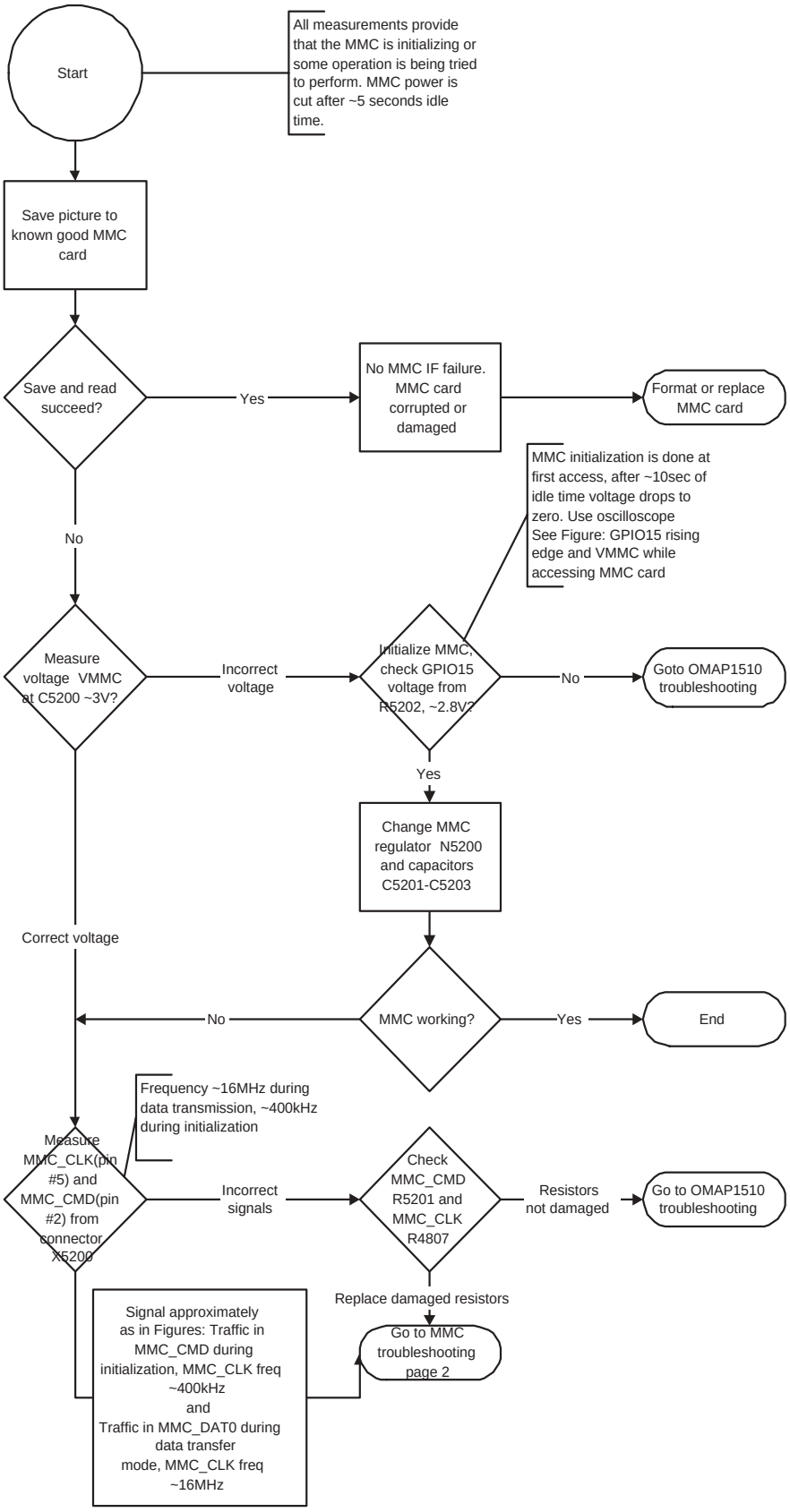
Start
All measurements provide that the MMC is initializing or some operation is being tried to perform. MMC power is cut after ~5 seconds idle time.
Save picture to known good MMC card
Save and read succeed?
Yes
No MMC IF failure. MMC card corrupted or damaged
Format or replace MMC card
MMC initialization is done at first access, after ~10sec of idle time voltage drops to zero. Use oscilloscope See Figure: GPIO15 rising edge and VMMC while accessing MMC card
No
Measure voltage VMMC at C5200 ~3V?
Incorrect voltage
Initialize MMC, check GPIO15 voltage from R5202, ~2.8V?
No
Goto OMAP1510 troubleshooting
Yes
Change MMC regulator N5200 and capacitors C5201-C5203
Correct voltage
MMC working?
No
Yes
End
Frequency ~16MHz during data transmission, ~400kHz during initialization
Measure MMC_CLK(pin #5) and MMC_CMD(pin #2) from connector X5200
Incorrect signals
Check MMC_CMD R5201 and MMC_CLK R4807
Resistors not damaged
Go to OMAP1510 troubleshooting
Replace damaged resistors
Go to MMC troubleshooting page 2
Signal approximately as in Figures: Traffic in MMC_CMD during initialization, MMC_CLK freq ~400kHz and Traffic in MMC_DAT0 during data transfer mode, MMC_CLK freq ~16MHz

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Figure 59:MMC troubleshooting (2/2)

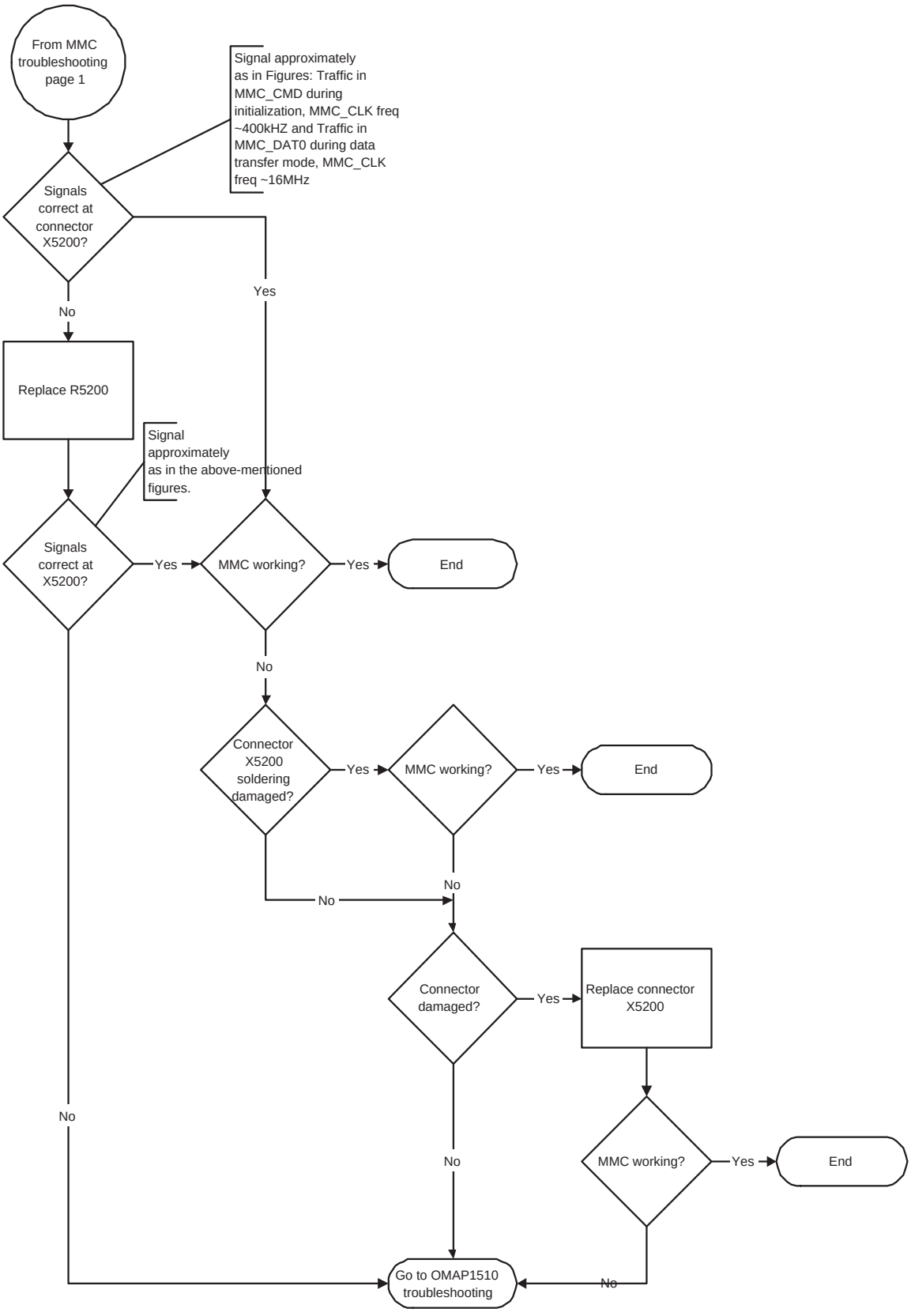

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Figure 60:GPIO15 rising edge and VMMC while accessing MMC card

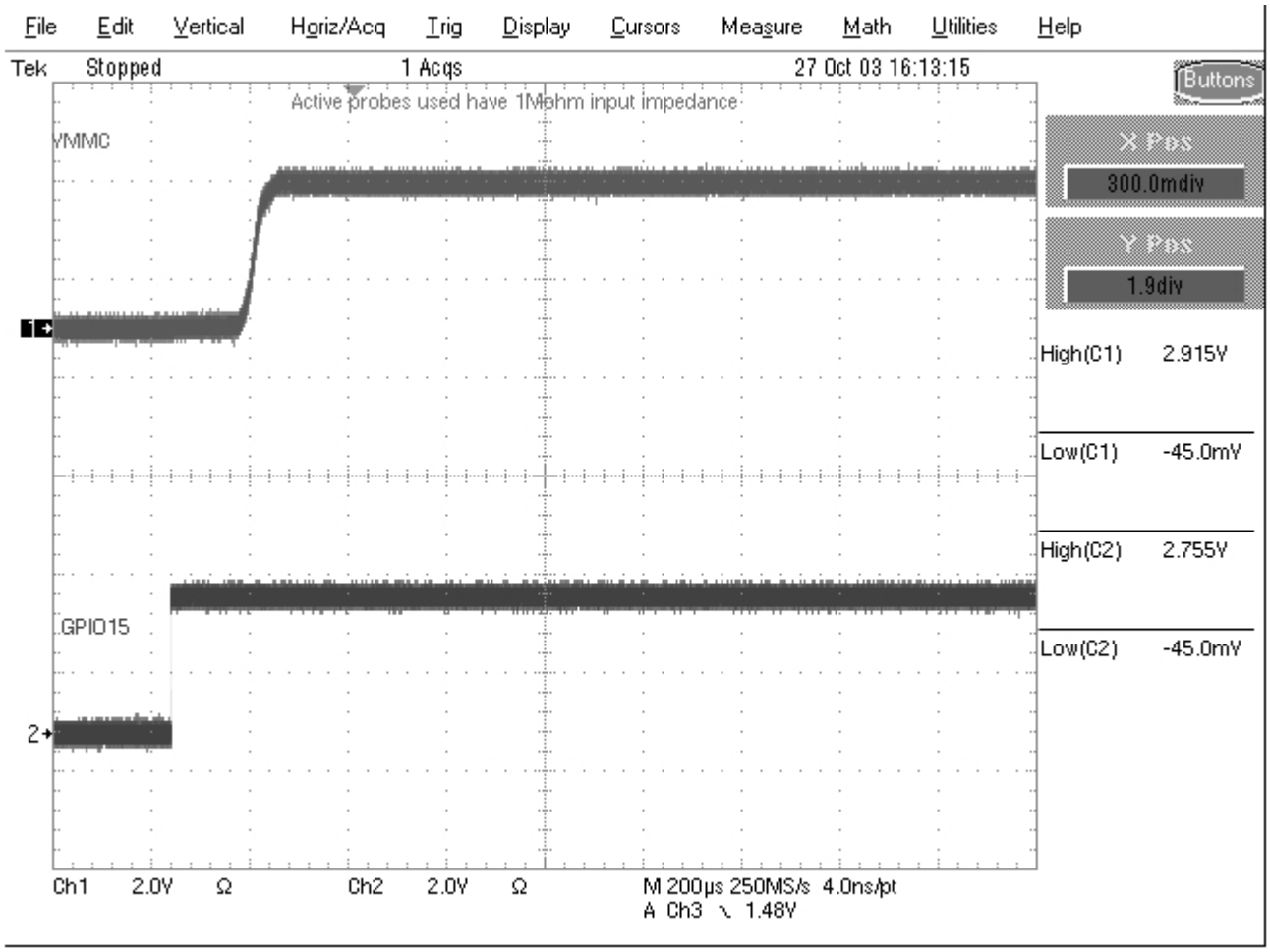

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Figure 61:Traffic in MMC_CMD during initialization, MMC_CLK freq ~400kHZ

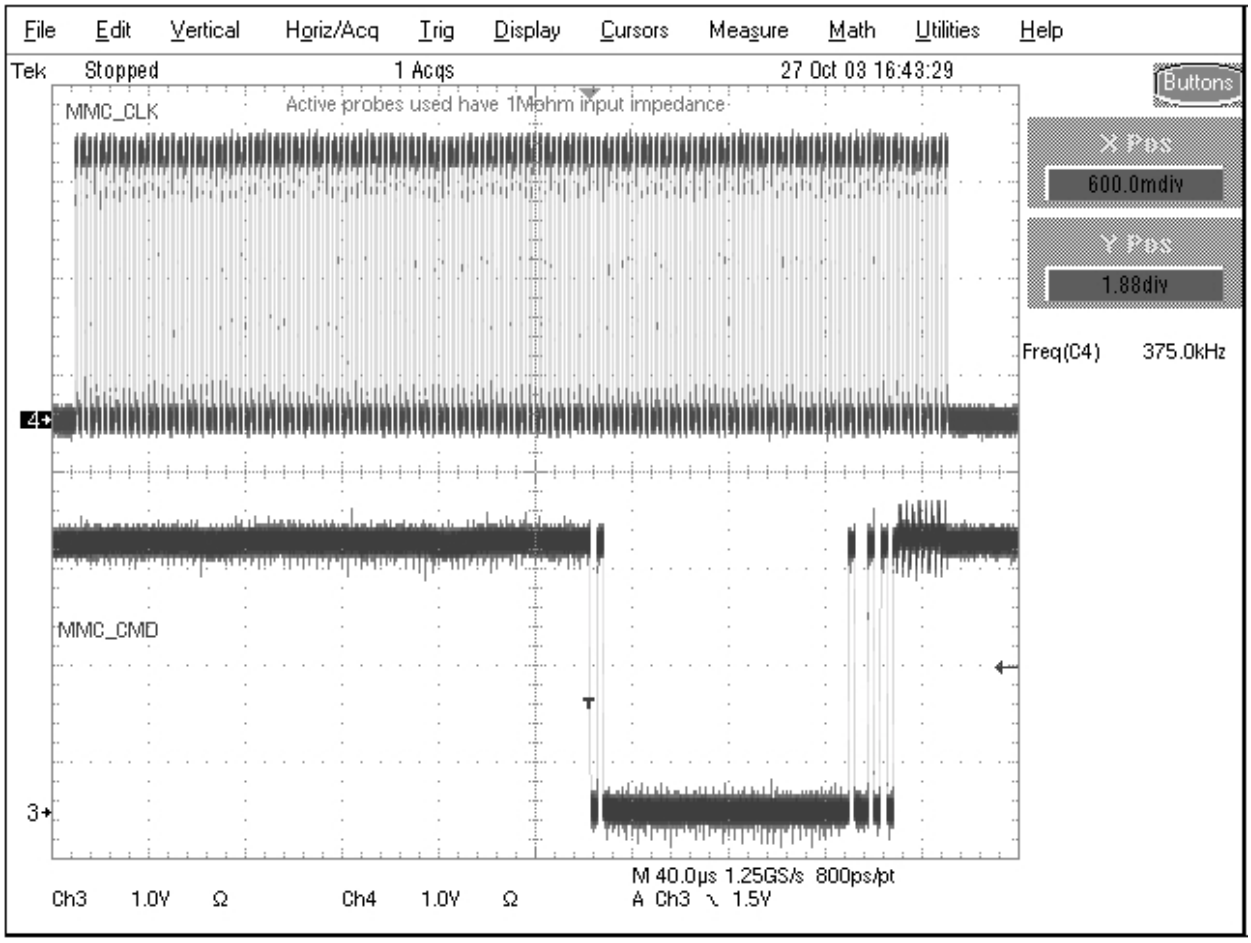

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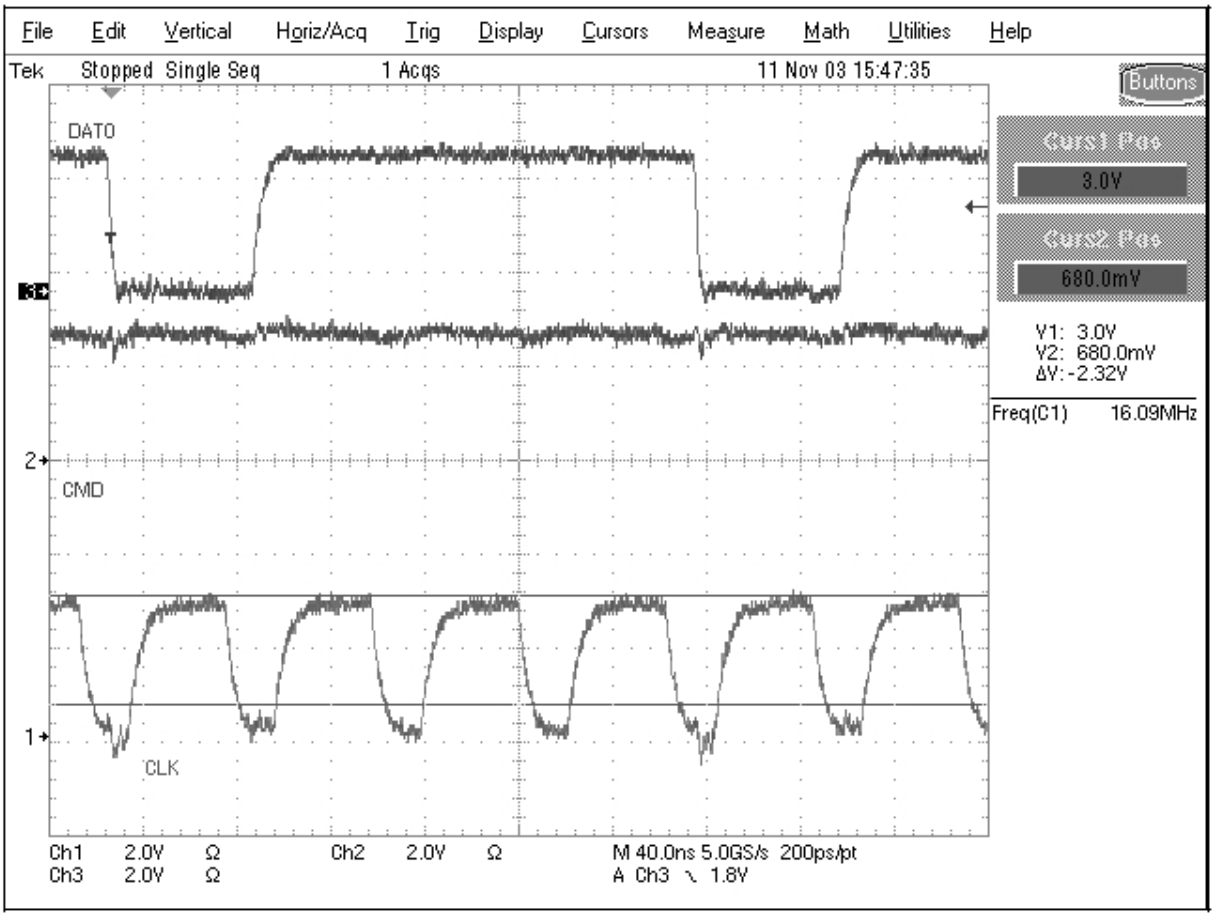
Figure 62:Traffic in MMC_DAT0 during data transfer mode, MMC_CLK freq ~16MHz



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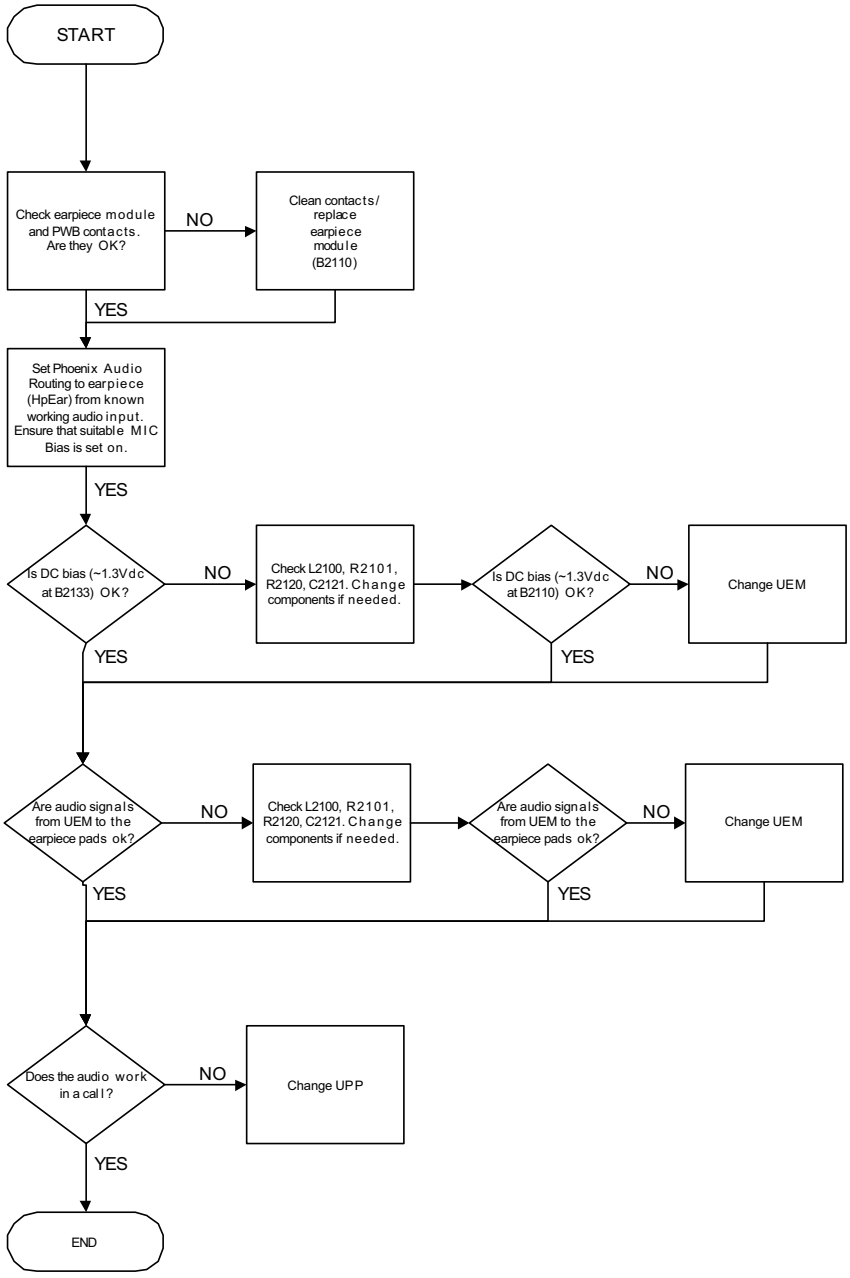
Audio faults

HP earpiece failure


START
Check earpiece module and PWB contacts. Are they OK?
NO
Clean contacts/ replace earpiece module (B2110)
YES
Set Phoenix Audio Routing to earpiece (HpEar) from known working audio input. Ensure that suitable MIC Bias is set on.
YES
Is DC bias (~1.3Vdc at B2133) OK?
NO
Check L2100, R2101, R2120, C2121. Change components if needed.
Is DC bias (~1.3Vdc at B2110) OK?
NO
Change UEM
YES
YES
Are audio signals from UEM to the earpiece pads ok?
NO
Check L2100, R2101, R2120, C2121. Change components if needed.
Are audio signals from UEM to the earpiece pads ok?
NO
Change UEM
YES
YES
Does the audio work in a call?
NO
Change UPP
YES
END

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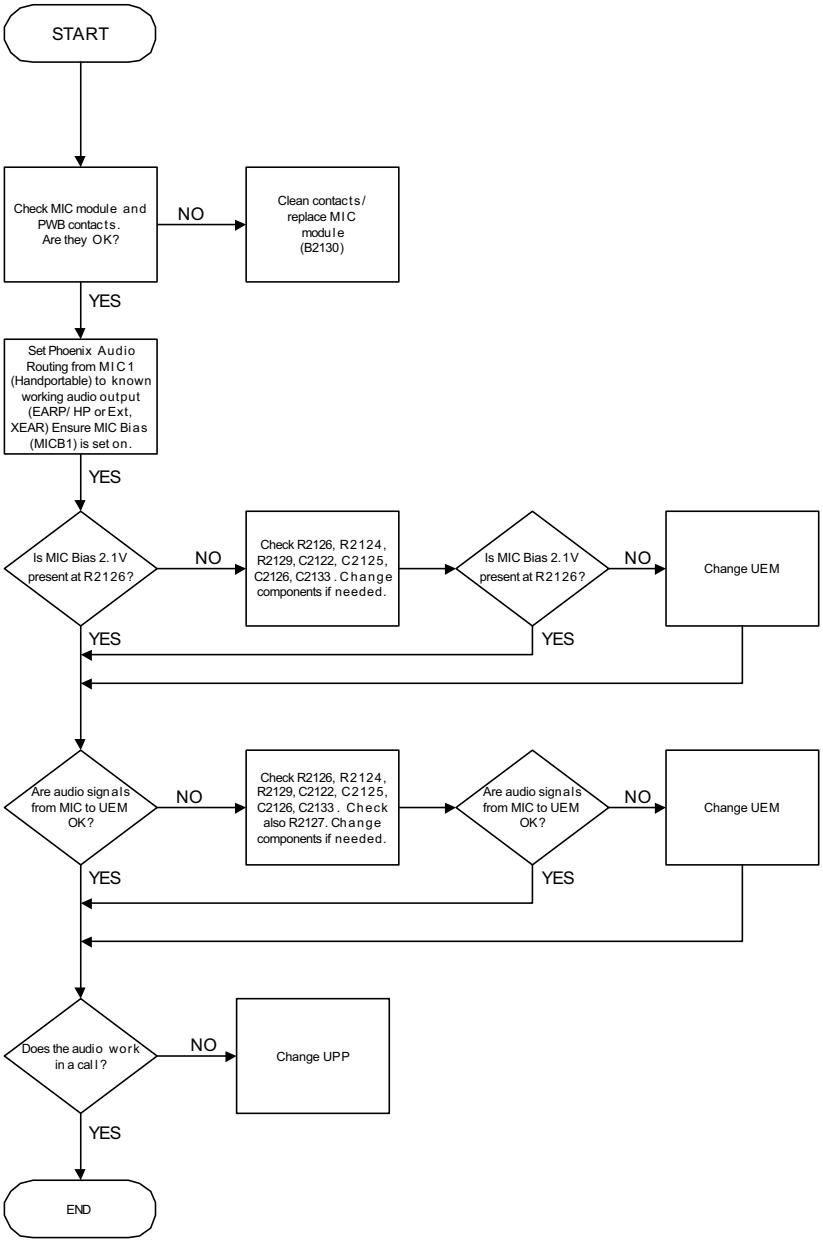
HP microphone failure


START
Check MIC module and PWB contacts. Are they OK?
NO
Clean contacts / replace MIC module (B2130)
YES
Set Phoenix Audio Routing from MIC1 (Handportable) to known working audio output (EARP/ HP or Ext, XEAR) Ensure MIC Bias (MICB1) is set on.
YES
Is MIC Bias 2.1V present at R2126?
NO
Check R2126, R2124, R2129, C2122, C2125, C2126, C2133. Change components if needed.
Is MIC Bias 2.1V present at R2126?
NO
Change UEM
YES
YES
Are audio signals from MIC to UEM OK?
NO
Check R2126, R2124, R2129, C2122, C2125, C2126, C2133. Check also R2127. Change components if needed.
Are audio signals from MIC to UEM OK?
NO
Change UEM
YES
YES
Does the audio work in a call?
NO
Change UPP
YES
END

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External earpiece failure

Figure 63:External earpiece failure (1/2)

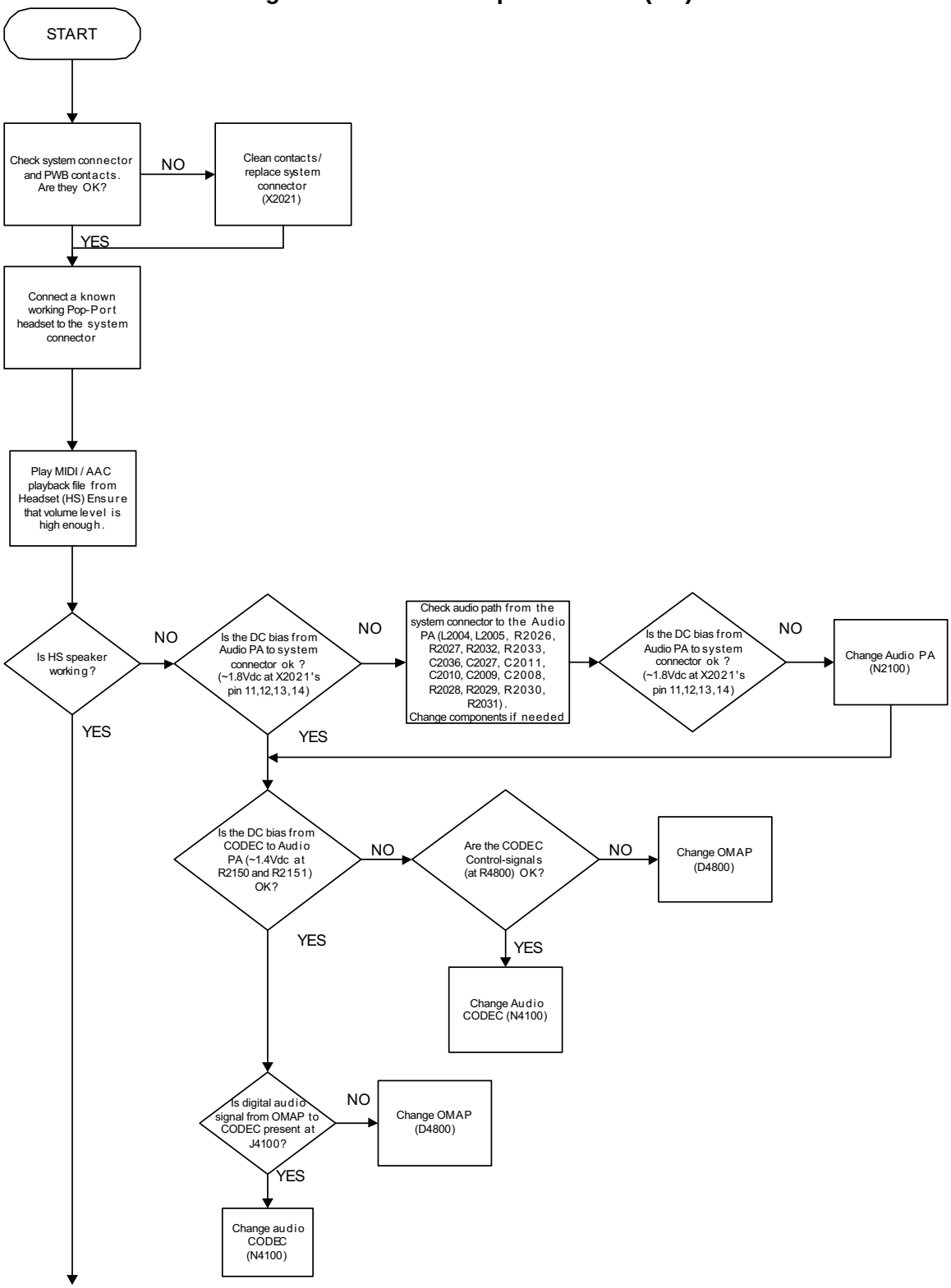
START
Check system connector and PWB contacts. Are they OK?
NO
Clean contacts / replace system connector (X2021)
YES
Connect a known working Pop-Port headset to the system connector
Play MIDI / AAC playback file from Headset (HS) Ensure that volume level is high enough.
Is HS speaker working?
NO
Is the DC bias from Audio PA to system connector ok ? (~1.8Vdc at X2021's pin 11,12,13,14)
NO
Check audio path from the system connector to the Audio PA (L2004, L2005, R2026, R2027, R2032, R2033, C2036, C2027, C2011, C2010, C2009, C2008, R2028, R2029, R2030, R2031). Change components if needed
Is the DC bias from Audio PA to system connector ok ? (~1.8Vdc at X2021's pin 11,12,13,14)
NO
Change Audio PA (N2100)
YES
YES
Is the DC bias from CODEC to Audio PA (~1.4Vdc at R2150 and R2151) OK?
NO
Are the CODEC Control-signals (at R4800) OK?
NO
Change OMAP (D4800)
YES
YES
Change Audio CODEC (N4100)
Is digital audio signal from OMAP to CODEC present at J4100?
NO
Change OMAP (D4800)
YES
Change audio CODEC (N4100)

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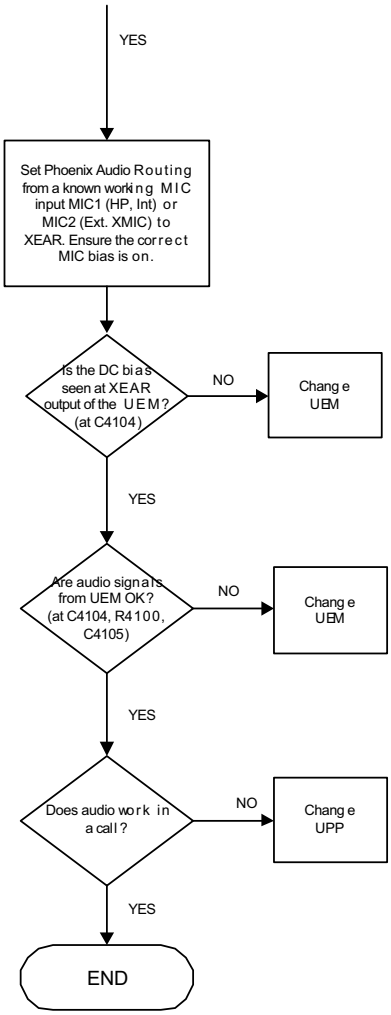
Figure 64:External earpiece failure (2/2)


YES
Set Phoenix Audio Routing from a known working MIC input MIC1 (HP, Int) or MIC2 (Ext. XMIC) to XEAR. Ensure the correct MIC bias is on.
Is the DC bias seen at XEAR output of the UEM? (at C4104)
NO
Change UEM
YES
Are audio signals from UEM OK? (at C4104, R4100, C4105)
NO
Change UEM
YES
Does audio work in a call?
NO
Change UPP
YES
END

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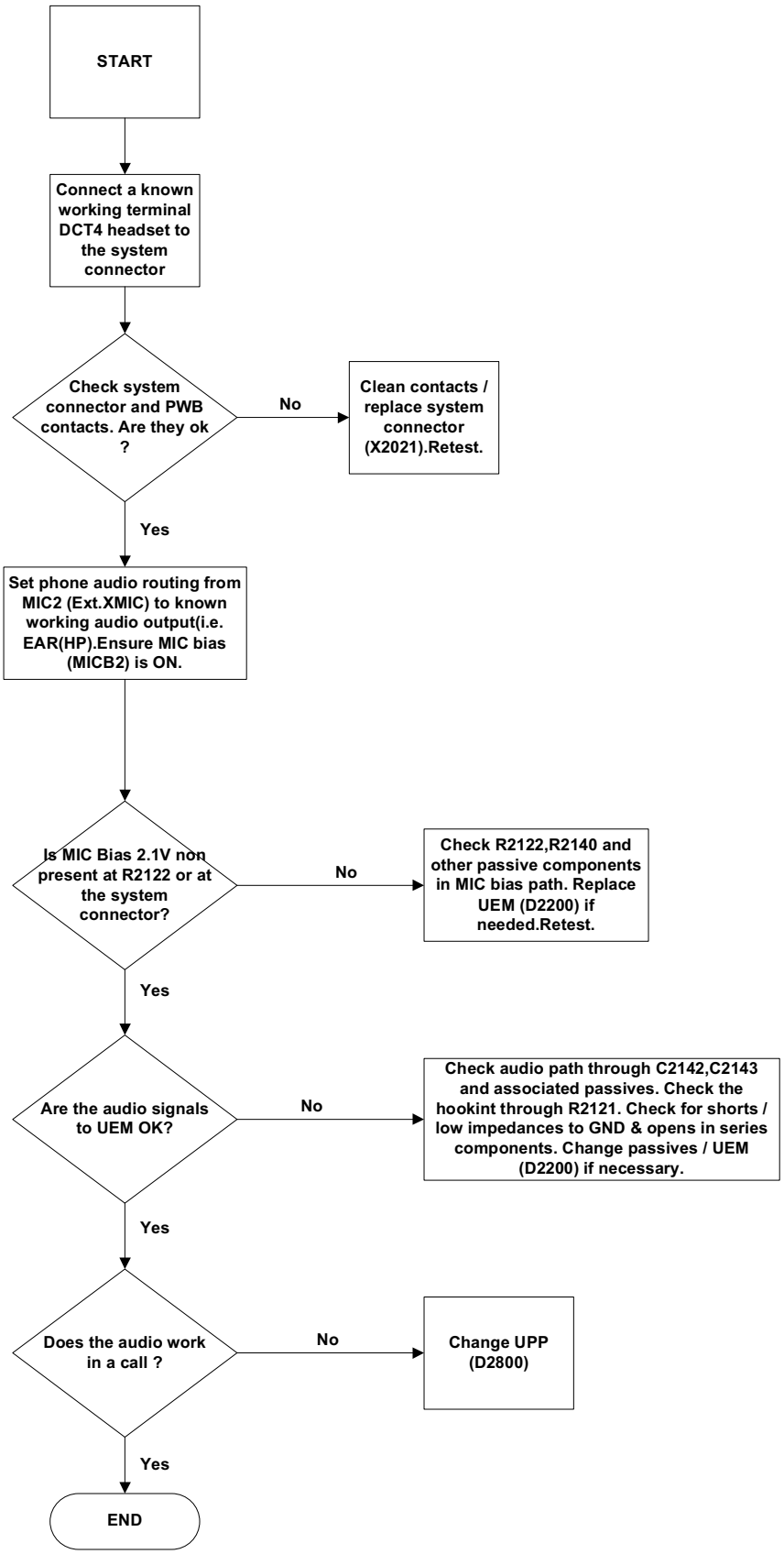
External microphone failure


START
Connect a known working terminal DCT4 headset to the system connector
Check system connector and PWB contacts. Are they ok ?
No
Clean contacts / replace system connector (X2021).Retest.
Yes
Set phone audio routing from MIC2 (Ext.XMIC) to known working audio output(i.e. EAR(HP).Ensure MIC bias (MICB2) is ON.
Is MIC Bias 2.1V non present at R2122 or at the system connector?
No
Check R2122,R2140 and other passive components in MIC bias path. Replace UEM (D2200) if needed.Retest.
Yes
Are the audio signals to UEM OK?
No
Check audio path through C2142,C2143 and associated passives. Check the hookint through R2121. Check for shorts / low impedances to GND & opens in series components. Change passives / UEM (D2200) if necessary.
Yes
Does the audio work in a call ?
No
Change UPP (D2800)
Yes
END

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IHF speaker failure

Figure 65:IHF speaker failure (1/2)

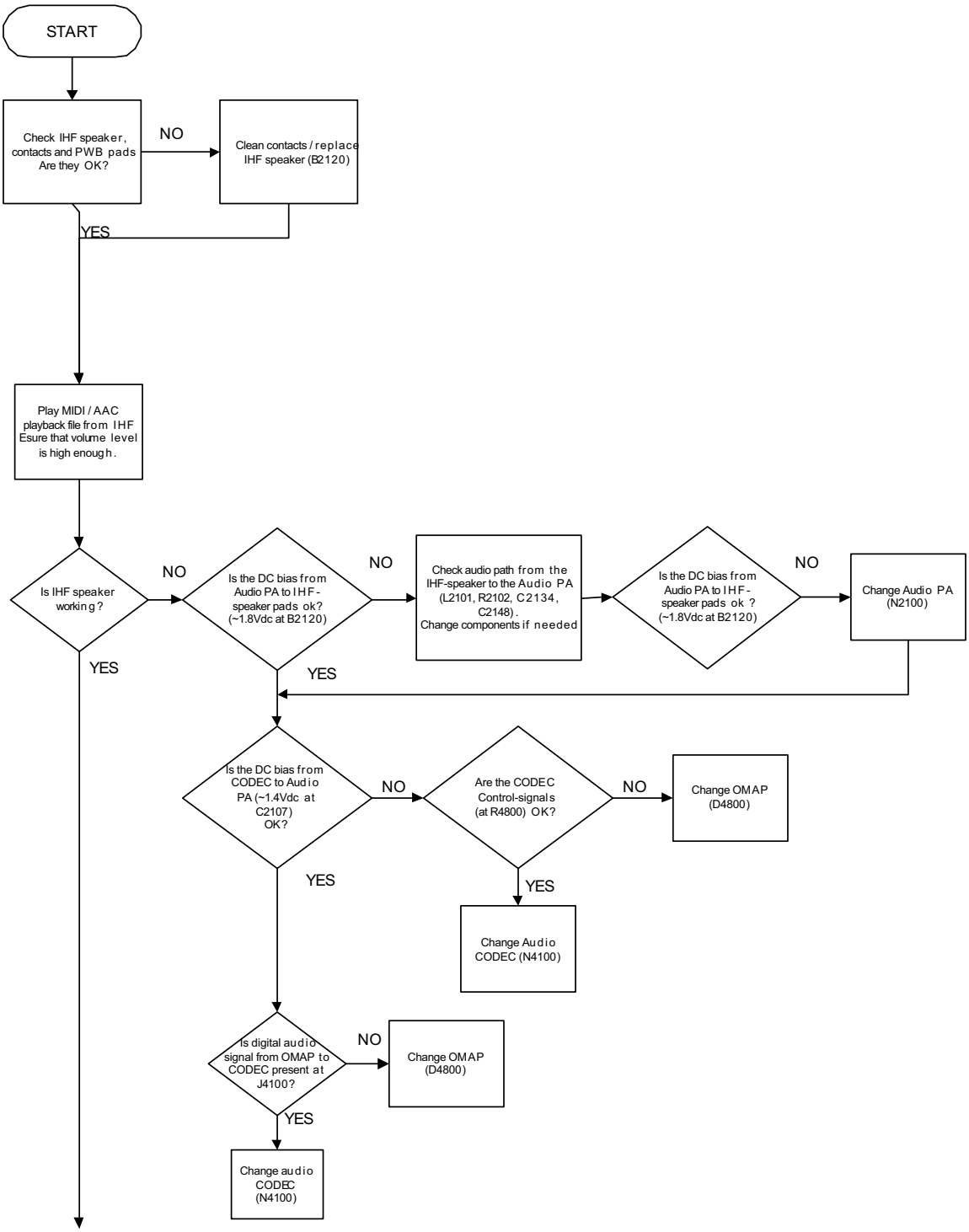
START
Check IHF speaker, contacts and PWB pads Are they OK?
NO
Clean contacts / replace IHF speaker (B2120)
YES
Play MIDI / AAC playback file from IHF Esure that volume level is high enough.
Is IHF speaker working?
NO
Is the DC bias from Audio PA to IHF-speaker pads ok? (~1.8Vdc at B2120)
NO
Check audio path from the IHF-speaker to the Audio PA (L2101, R2102, C2134, C2148). Change components if needed
Is the DC bias from Audio PA to IHF-speaker pads ok ? (~1.8Vdc at B2120)
NO
Change Audio PA (N2100)
YES
YES
Is the DC bias from CODEC to Audio PA (~1.4Vdc at C2107) OK?
NO
Are the CODEC Control-signals (at R4800) OK?
NO
Change OMAP (D4800)
YES
YES
Change Audio CODEC (N4100)
Is digital audio signal from OMAP to CODEC present at J4100?
NO
Change OMAP (D4800)
YES
Change audio CODEC (N4100)

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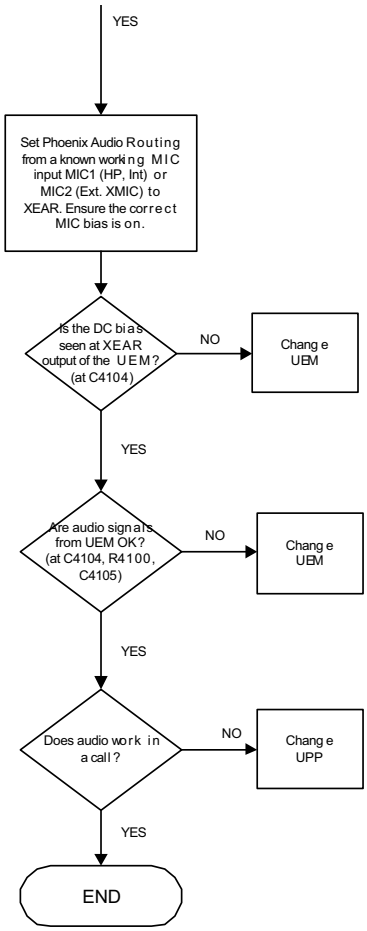
Figure 66:IHF speaker failure (2/2)


YES
Set Phoenix Audio Routing from a known working MIC input MIC1 (HP, Int) or MIC2 (Ext. XMIC) to XEAR. Ensure the correct MIC bias is on.
Is the DC bias seen at XEAR output of the UEM? (at C4104)
NO
Change UEM
YES
Are audio signals from UEM OK? (at C4104, R4100, C4105)
NO
Change UEM
YES
Does audio work in a call?
NO
Change UPP
YES
END

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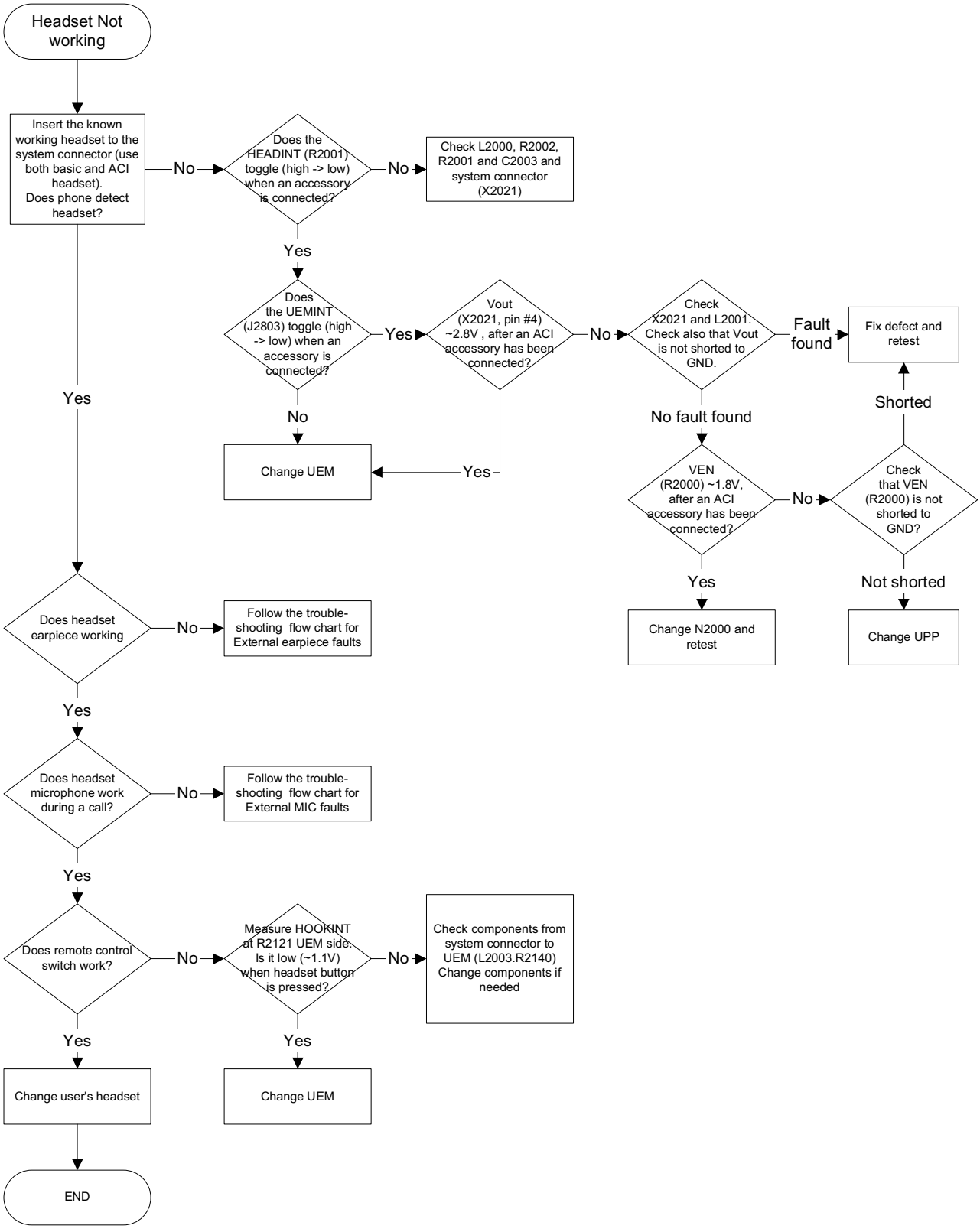
Accessory detection troubleshooting

Figure 67: General accessory troubleshooting


Headset Not working
Insert the known working headset to the system connector (use both basic and ACI headset). Does phone detect headset?
No
Does the HEADINT (R2001) toggle (high -> low) when an accessory is connected?
No
Check L2000, R2002, R2001 and C2003 and system connector (X2021)
Yes
Does the UEMINT (J2803) toggle (high -> low) when an accessory is connected?
Yes
Vout (X2021, pin #4) ~2.8V , after an ACI accessory has been connected?
No
Check X2021 and L2001. Check also that Vout is not shorted to GND.
Fault found
Fix defect and retest
Shorted
No fault found
No
Change UEM
Yes
Yes
VEN (R2000) ~1.8V, after an ACI accessory has been connected?
No
Check that VEN (R2000) is not shorted to GND?
Yes
Not shorted
Change N2000 and retest
Change UPP
Yes
Does headset earpiece working
No
Follow the trouble-shooting flow chart for External earpiece faults
Yes
Does headset microphone work during a call?
No
Follow the trouble-shooting flow chart for External MIC faults
Yes
Does remote control switch work?
No
Measure HOOKINT at R2121 UEM side. Is it low (~1.1V) when headset button is pressed?
No
Check components from system connector to UEM (L2003.R2140) Change components if needed
Yes
Yes
Change user's headset
Change UEM
END

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Camera module troubleshooting

Faults associated with camera operation can be roughly categorised into three subgroups:

- Camera is not functional at all, no image can be taken
- Images can be taken but there is nothing recognisable in them
- Images can be taken and they are recognisable but for some reason the quality of the images is seriously degraded

Image quality is very hard to measure quantitatively, and even comparative measurements are difficult (comparing two images), if the difference is small. Especially if the user is not satisfied with his/her device's image quality, and tells e.g. that the images are not sharp, it is very difficult to test the device and get an exact figure which then would tell if the device is OK or not.

Often, subjective evaluation has to be used in order to find out if a certain property of the camera is acceptable or not. Some training and a correctly operating reference device may be needed in order to detect what actually is wrong, or whether there is anything wrong at all. It is easy for the user to take images of poor quality in bad conditions. Therefore the camera operation has to be checked always in constant conditions (lighting, temperature) or by using a second, known-to-be good device as a reference.

Terms

Dynamic range: the camera's ability to capture details in dark and bright areas of the scene simultaneously.

Exposure time: camera modules use a silicon sensor to collect light and to form an image. The imaging process roughly corresponds to traditional film photography, in which exposure time means the time during which the film is exposed to the light coming through optics. Increasing the time allows more light hitting the film and thus resulting in brighter image. The operation principle is exactly the same with the silicon sensor, but the shutter functionality is handled electronically, i.e. there is no mechanical moving parts like in film cameras.

Flicker: a phenomenon, which is caused by pulsating in scene lighting, typically appearing as wide horizontal stripes in image.

Noise: variation of response between pixels with same level of input illumination.

Image taking conditions effect on image quality

This chapter lists some of the factors, which may cause poor image quality if not taken into account, and thus result in complaints from customers.

Several issues affect the image quality and needs to be taken into account when shooting pictures; the listed items are normal to camera operation:

Distance to target: the lens in the module is specified to operate satisfactorily from 30 cm to infinite distance of scene objects. In practice, the operation is such that close objects may be noticed to get more blurred when distance is less than 40cm. The lack of sharpness is first visible in full resolution (VGA) images. If just observing the viewfinder, even very close objects may seem to appear sharp.

Sharpness of picture edges: lens performance degrades on the image edges, and generally the image is sharpest at the centre. Particularly, this applies to distant objects (> 1 meter). See Figure 1, "Sharpness of the picture is worse on the edges than at the centre," below.

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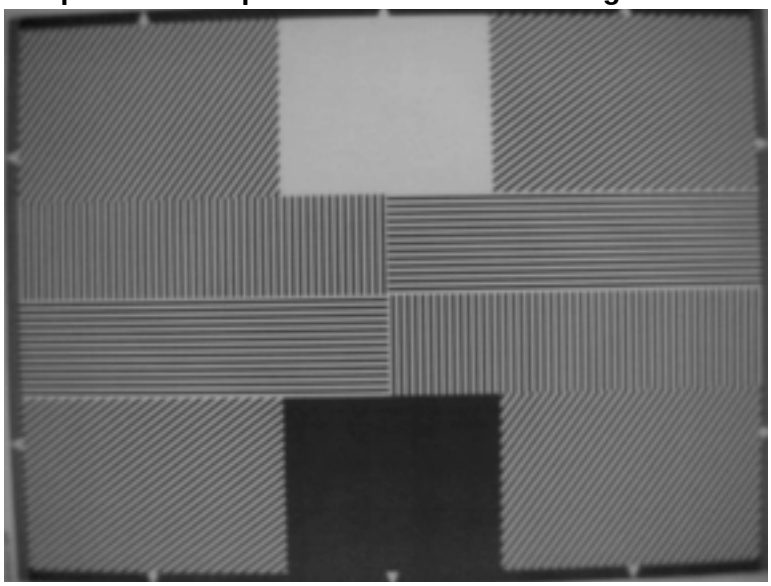
Figure 1: Sharpness of the picture is worse on the edges than at the centre



Geometrical distortion: camera lens causes some amount of so called barrel distortion. In practice, this appears as bending of straight objects on the edges of the image. See the following picture (wall in the background).

Amount of light available: in dim conditions camera runs out of sensitivity. The exposure time is long (especially in night mode) and the risk of getting shaken images increases. Image noise level grows. The maximum exposure time in the night mode is approximately ¼ seconds, so images need to be taken with extreme care when the amount of light reflected from the target is low.

Figure 2:shaking hands caused blurring of this image.

Note! geometrical barrel distortion in the background

Movement in bright light: If pictures of moving objects are taken or if the device is used, for example, in a moving car, object 'skewing' or 'tilting' may occur. This phenomena is fundamen-

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tal and normal to most CMOS camera types and therefore cannot be fixed in any way. Movement of camera or object usually causes blurring indoors or in dim lighting conditions due to the long exposure time.

Figure 3:Near objects in the image get skewed when shooting from a moving car

Temperature: high temperatures inside the mobile phone cause more noise to appear in images, e.g. in +70 degrees of celsius the noise level may be very high, and it further grows if the conditions are dim. This is also normal as regards the camera operation.

Figure 4:Noisy image taken in +70 deg

Display: if the display contrast is set too dark, the image quality degrades: the images may be very dark, depending on the setting. This problem is easily solved by setting the display contrast to the correct value.

Basic rules of photography, especially shooting against light: electronic image sensors typically have much lower dynamic range than films. In practice this means that when taking a picture indoors, e.g. having a window behind object, leads to poor results.

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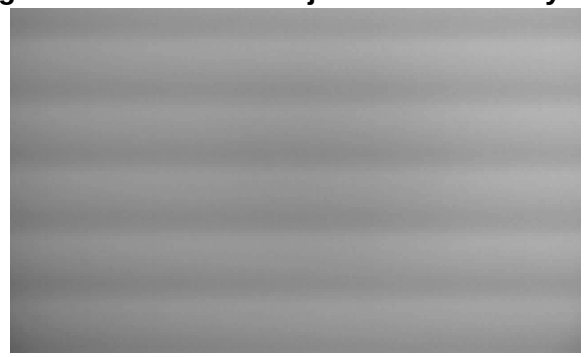
Figure 5:Image which has been taken "against the light". The actual object (a squirrel) cannot be seen well.

Flicker: in some rare occasions a very bright fluorescent light may cause flicker in the viewfinder image.

Figure 6:Flicker in image of white uniform object illuminated by strong fluorescent light



Bright light outside image view: Especially sunlight can cause clearly visible 'halo' effects and poor contrast in images. The light produces undesired reflections inside camera optics.

Figure 7:A lens reflection effect caused by sun shining above the scene

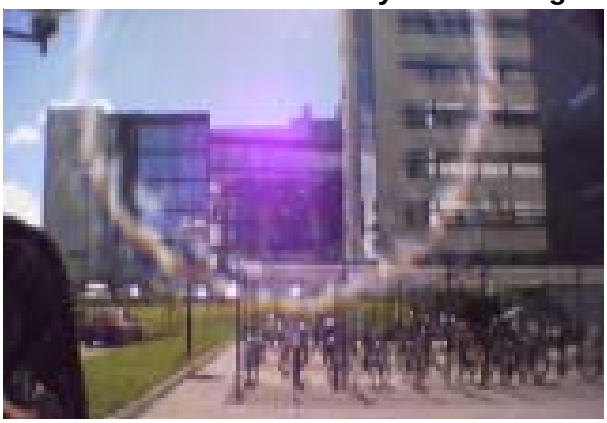


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Figure 8:A good quality picture taken indoors

Note:The camera module as a component is not a repairable part i.e. components in the module may not be changed. Cleaning dust from the front face is the only allowable operation.

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Camera hardware failure message

Figure 9:Camera hardware failure (1/2)

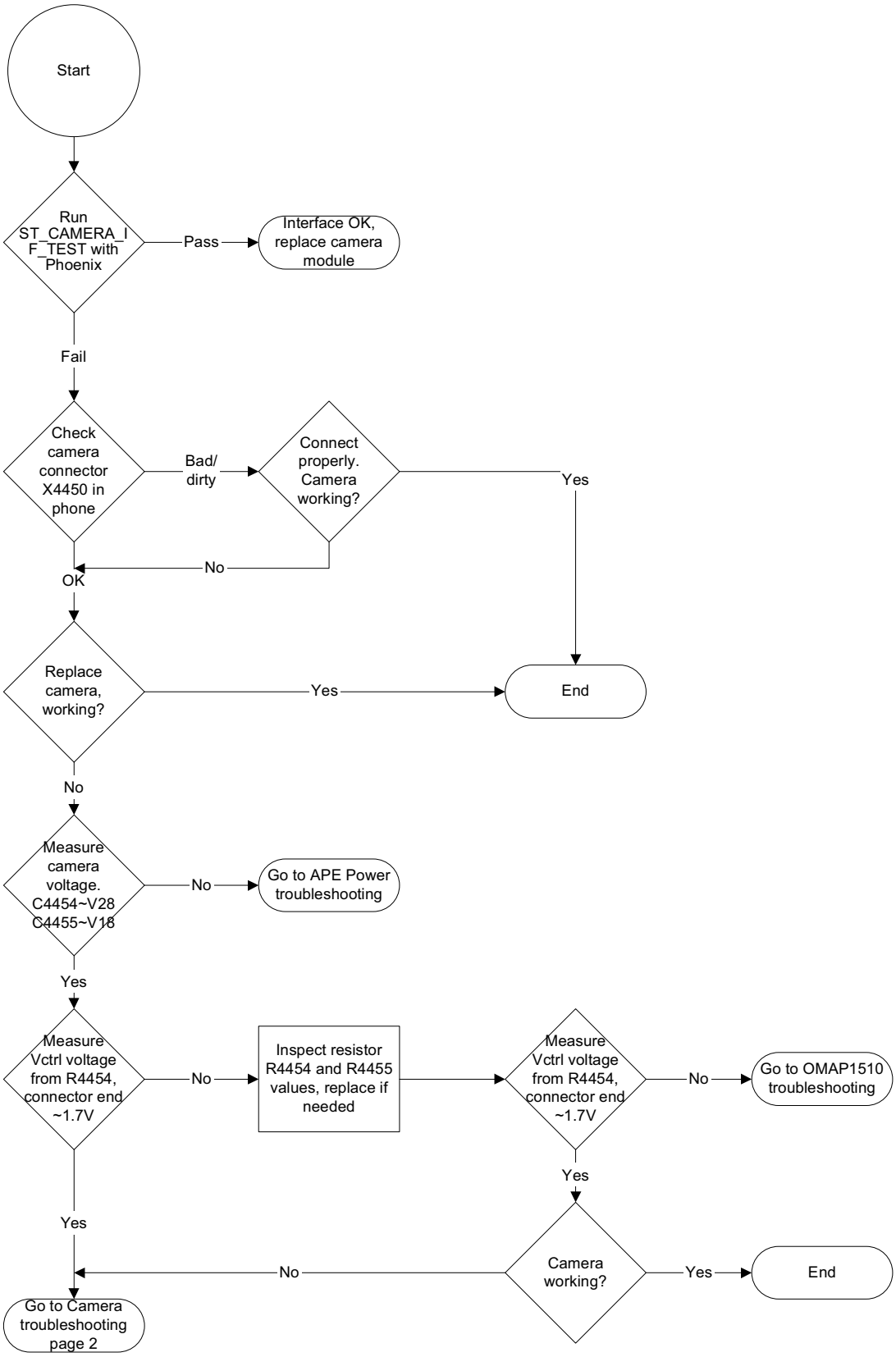

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Figure 10:Camera hardware failure (2/2)

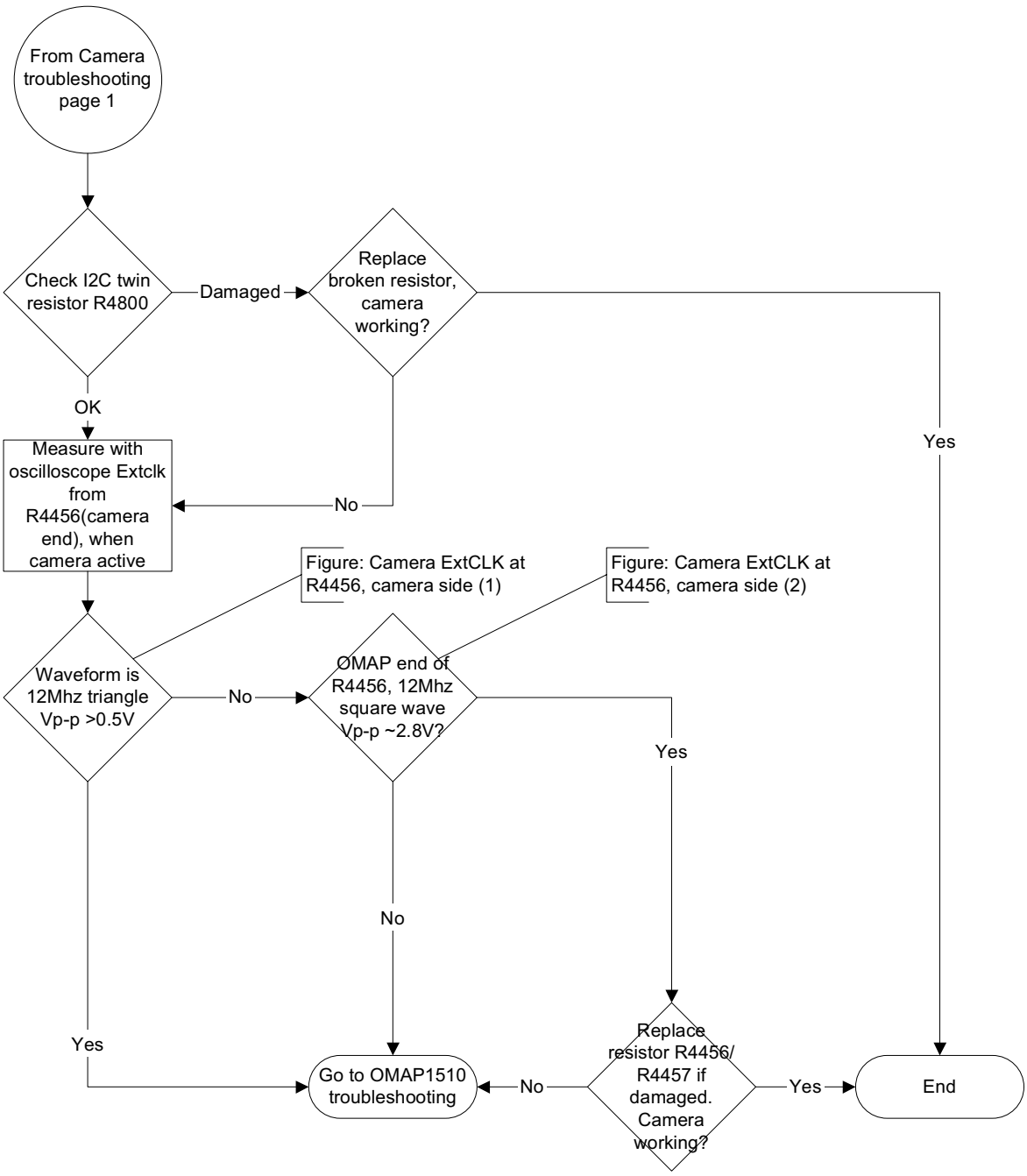

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Figure 11:Camera ExtCLK at R4456, camera side (1)

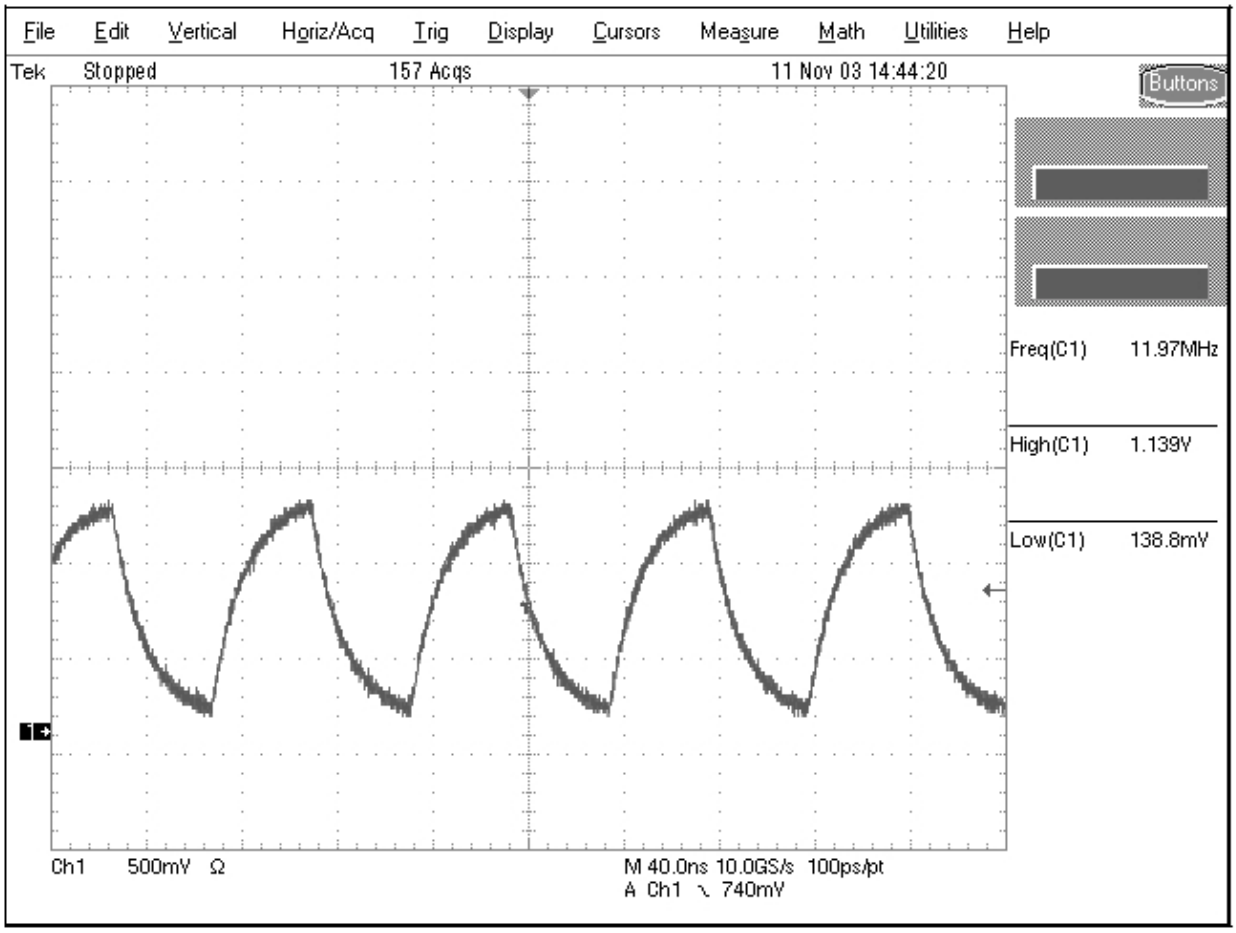

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Figure 12:Camera ExtCLK at R4456, camera side (2)

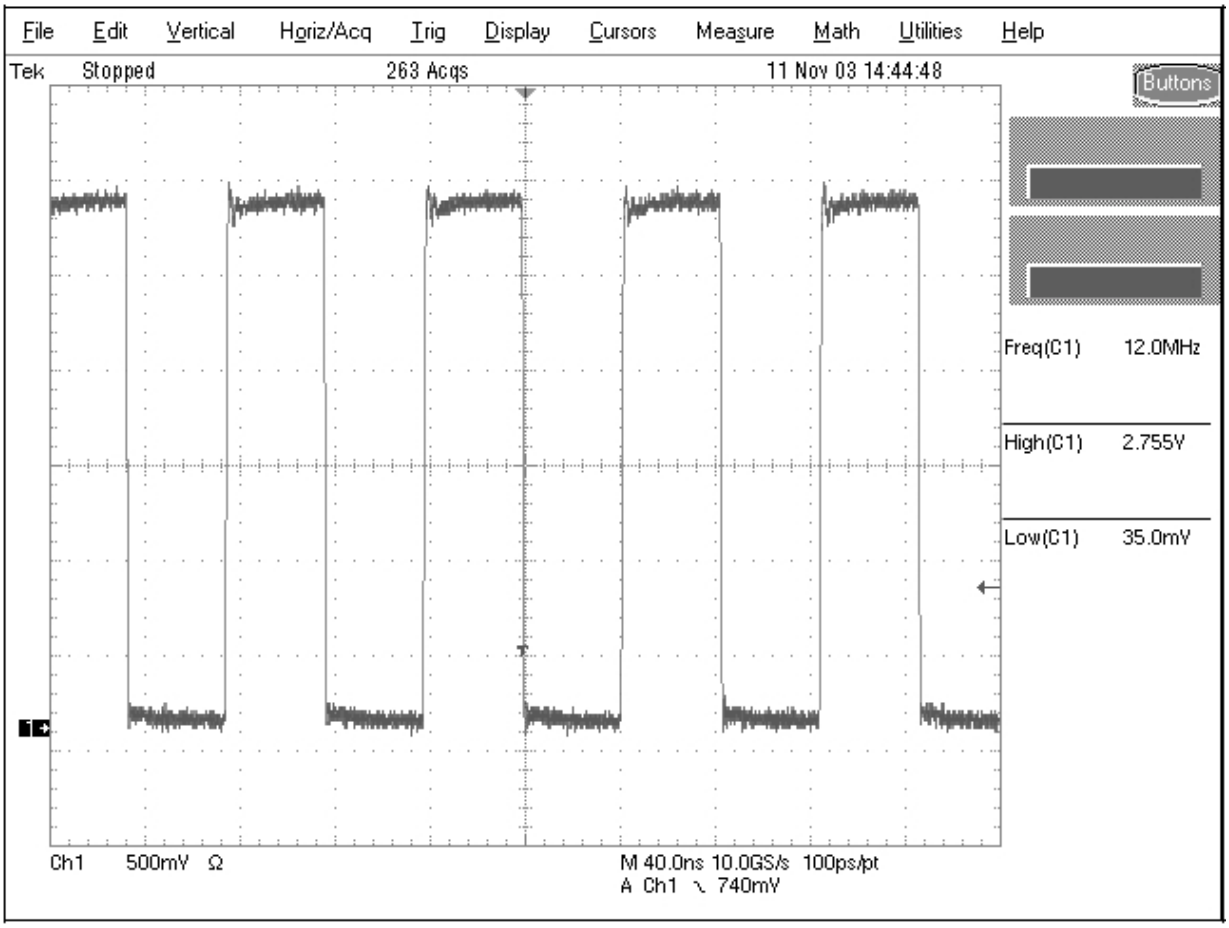
File Edit Vertical Horiz/Acq Trig Display Cursors Measure Math Utilities Help
Tek Stopped 263 Acqs 11 Nov 03 14:44:48
Buttons
Freq(C1) 12.0MHz
High(C1) 2.755V
Low(C1) 35.0mV
Ch1 500mV Ω
M 40.0ns 10.0GS/s 100ps/pt
A Ch1 ∖ 740mV

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Image quality analysis

Possible faults in image quality

When checking possible errors in the camera functionality, knowing what error is suspected significantly helps the testing by narrowing down the amount of test cases. The following types of image quality problems may be expected to appear (in order of appearance probability):

- Dust (black spots)
- Lack of sharpness
- Bit errors

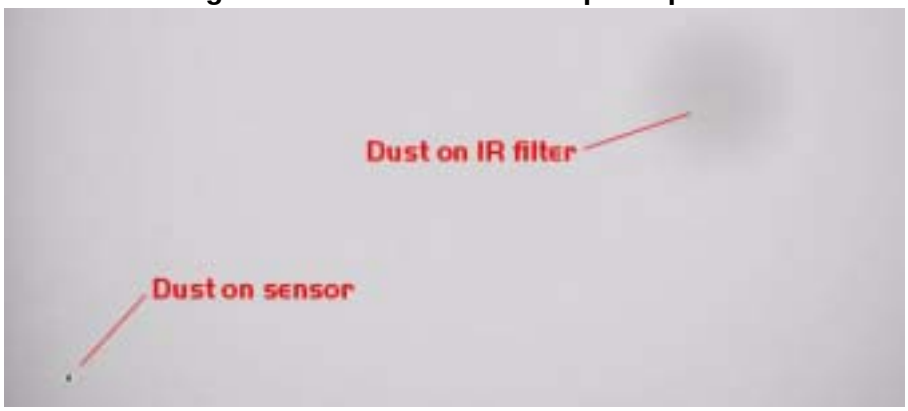
Testing for dust

For detecting this kind of problem, take an image of a uniform white surface and analyse it in full resolution; search carefully – finding these defects is not always easy. Figure 13, “Effects of dust in optical path,” is an example of an image containing easily detectable dust problems.

Black spots in the image are caused by dirt particles trapped into the optical system: clearly visible and sharp edged black dots in image are typically dust particles on image sensor. These spots are searched for in the manufacturing phase, but it is possible that the lens holder cavity contains a particle, which may move onto the image sensor active surface, e.g. when the phone is dropped. Thus it is also possible that the problem disappears before the phone is brought to service. The camera should be replaced if it has been in some phase *verified* that the problem has been present.

If dust particles are located on the infrared filter surface on either side, they are much harder to locate because they are out of focus, and appear in image as large, greyish and fading-edge 'blobs'. Sometimes they are very hard to find, and thus the user probably does not notice them at all since they do no harm. But it is possible that a larger particle disturbs the user, causing need for service.

Figure 13:Effects of dust in optical path



If large dust particles get trapped on top of the lens surface in the cavity between camera window and lens, they may cause image blurring and poor contrast (see also item 'sharpness'). The seal between the window and lens should prevent any particles from getting into the cavity after the manufacturing phase.

If dust particles are found on sensor or are suspected to be inside the camera module, this is classified as a manufacturing error of the module and thus the camera should be replaced. The particles inside the cavity between the window and the lens are most probably been trapped there in the assembly phase at a Nokia factory. It is of course also possible that the user has

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disassembled the device and caused the problem. However, in most cases it should be possible to remove the particle(s) by using compressed air. Never wipe the lens surface before trying compressed air; the possibility of damaging the lens is substantial. Always check the image sharpness after removing dust.

Testing for sharpness

If pictures taken with a phone are claimed to be blurry, there are five possible sources for the claim:

- User has tried to take pictures in too dark conditions and images are blurred due to handshake or movement. This is not a reason to replace camera module.
- There is dirt between back window and camera lens.
- The back window is defective (somehow passed through window manufacturer's inspection). Window should be changed.
- The back window is visibly scratched, broken or dirty.
- Camera lens is misfocused.

Quantitative analysis of sharpness is very difficult to conduct in other than optics laboratory environment. Thus subjective analysis should be used.

If no visible defects (items 2-4) can be found, a couple of test images should be taken and checked. Generally, a well-illuminated typical indoor office scene, such as the one in Figure 8, “A good quality picture taken indoors,” on page 137, can be used as a target. The main considerations are:

- The amount of light: 300 – 600 lux (bright office lighting) is sufficient.
- The scene should contain small objects for checking the sharpness and the distance to them should be in order of 1 – 2 meters.
- If possible, compare the image to another image of the same scene, taken with a different device.

The taken images should be analysed on a PC screen at 100% scaling simultaneously with the reference image. Pay attention to the computer display settings; at least 65000 colours (16 bit) have to be used. 256 (8-bit) colour setting is not sufficient. True colour (24 bit, 16 million colours) or 32 bit (full colour) setting is recommended.

If there appears to be a clearly noticeable difference between the reference image and the test image, the module might have a misfocused lens. In this case, the module should be changed.

Always re-check the resolution after changing the camera. If a different module produces the same result, the fault is probably in the camera window. Check the window by looking through it when replacing the module.

Bit errors

Bit errors are defects in the image caused by a data transmission error between camera and the phone baseband. This type of error is expected to be rare since usually missing bits cause a hardware failure message. Bit errors can typically be seen in images taken of any object, and they should be most visible in full VGA resolution images. Viewfinder images may not contain the errors at all due to lower bit rate used in this mode. A good practice is to use uniform white test target.

The errors are clearly visible as colourful sharp dots or lines in camera VGA images.

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